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A Five Gigahertz Bandwidth Optical Receiver and Amplifier

BY

© **Thomas Michael Seniuk**

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of **Master of Science**.

DEPARTMENT OF **ELECTRICAL ENGINEERING**

Edmonton, Alberta
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For my parents, Nick and Edna Seniuk.

Abstract

A hybrid microwave integrated amplifier, suitable for use in a 10 Gbit/s communication system, is designed to achieve a bandwidth from a few MHz to 6 GHz and a gain of 20 dB. A low noise figure and low reflections at the input and output are also desired. In order to meet these goals, three stages of RC coupled low-noise microwave FETs known as high electron mobility transistors (HEMTs) in common source configuration are used. To extend the upper frequency 3 dB-down point, a technique known as inductive peaking is employed to achieve the wide bandwidth goal.

Empirical tuning techniques are used to alter the amplifier as designed to produce a flat gain response. Gain of 25 dB with less than 0.75 dB of ripple is measured up to the 3 dB-down point of 5.37 GHz. A second amplifier with measured gain of 24.5 dB and bandwidth of 5.1 GHz is constructed as well, therefore demonstrating a limited amount of reproduction potential.

The same amplifier topology is then used as the basis for an optical receiver. Linear arrays of GaAs metal-semiconductor-metal (MSM) photodetectors are used as the optical input to the receiver. The amplifier design is re-optimized to exhibit 50 dBΩ of transimpedance gain up to 10 GHz.

Adjustments are made to the optical receiver to achieve more than 40 dBΩ of transimpedance gain, but with 3 dB of gain ripple up to 5 GHz with any of the seven functioning MSMs of the array acting as inputs of the receiver, despite the previously known position-dependent frequency response of the MSM arrays [27]. This indicates the possibility of using GaAs MSM linear arrays in hybrid optical receivers for 10 Gbit/s optoelectronic switching and signal processing.

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List of Abbreviations

APD	avalanche photodiode
AMC	Alberta Microelectronics Centre
BNR	Bell-Northern Research
CRC	Communications Research Centre
CW	continuous wave
EMI	electromagnetic interference
Gbit/s	gigabits per second
HBT	heterojuction bipolar transistor
HEMT	high electron mobility transistor
HP	Hewlett-Packard
ISI	inter-symbol interference
MBE	molecular beam epitaxy
MDS	Microwave Design System
MESFET	metal-semiconductor field effect transistor
MIC	microwave integrated circuit
MMIC	monolithic microwave integratec circuit
MOCVD	metal-organic chemical vapor deposition
MSM	metal-semiconductor-metal
NRZ	non-return-to-zero
PD	photodiode or photodetector
SWR	standing wave ratio
TFB	transistor feedback block

1. Introduction

For long-haul telecommunication systems, fibre optic cable is the preferred transmission medium, over traditional coaxial cable. Glass fibre exhibits no crosstalk or electromagnetic interference (EMI), very low loss of 0.25 to 0.2 dB/km, and a virtually unlimited bandwidth. This results in improved transmission quality, reliability, and a higher channel capacity. In order to realize the capacity potential, which will be needed to meet ever-increasing voice and data traffic on telecommunication systems, long-distance carriers can either install more fibre trunks, which is an expensive option, or increase bit rates on existing fibre trunks to as high as multi-gigabits per second. In the near future, 10 Gbit/s optical transmission systems are expected to be the next step in speed. In order to transmit or receive these signals, optoelectronic components like laser diodes and photodetectors and electronic components such as multiplexers, demultiplexers, and amplifiers must operate well into the microwave spectrum, and with bandwidths that extend from a few megahertz to at least 5 GHz, assuming non-return-to-zero (NRZ) signaling. All the usual engineering requirements of relatively low initial cost, compactness, high reliability, and low maintenance costs apply.

This thesis will present the design, construction, and testing of one component of this high-speed system: a wideband optoelectronic receiver. The performance requirements of the electronic amplifier in this receiver were established at the outset. They were to achieve a gain of 20 dB with as little ripple as possible in the passband to meet low inter-symbol interference (ISI) requirements, and a bandwidth from a few megahertz up to 6 GHz, which is higher than the minimum 5 GHz requirement needed to ensure quality reproduction of a 10 Gbit/s signal. When configured as an optical receiver, a metal-semiconductor-metal (MSM) photodetector acts as the input to the amplifier. To meet the low cost requirement, noting that only one or two amplifiers are required, the circuit is constructed in hybrid, rather than monolithic integrated, form. Processing GaAs wafers using molecular beam epitaxy (MBE) or even metal-organic chemical vapor deposition (MOCVD) is an extremely expensive way to fabricate the small number of circuits required for experimental research. On the other hand, microwave chip transistors such as metal-semiconductor FETs (MESFETs) or high electron mobility transistors (HEMTs) are available commercially for a few tens of dollars apiece. Passive chip components, such as resistors and capacitors, are also cheap and available. A high-permittivity substrate on which the chip components are placed and interconnected and metal packaging are the only custom components required.

1.1 Design Options for Wideband Amplification

In the literature, many ways are described to meet the goals given on the preceding page. Almost anyone who has designed and/or built an amplifier such as this in the past chooses, as active devices, GaAs MESFET or HEMT transistors, in common source configuration. The circuit symbol and simple structure of a typical small-signal microwave MESFET are shown in Figure 1.1.

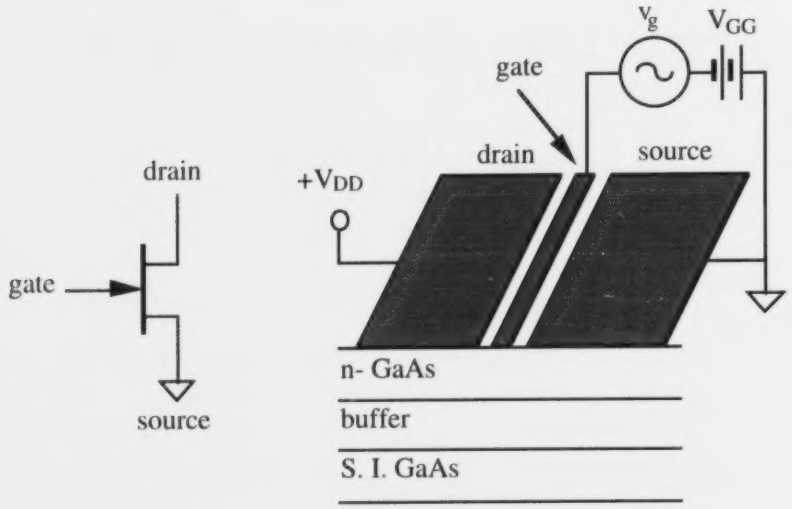


Figure 1.1 Schematic diagram and simple structure of a MESFET

Heterojunction bipolar transistors (HBTs), in discrete form, do not have enough gain as frequencies enter the multi-gigahertz range although they have been successfully used in a 2 GHz hybrid microwave integrated circuit (MIC) optical receiver [1].

Most designs incorporate three stages of active devices, capacitively coupled, to achieve 15 to 20 dB of gain, as in Figure 1.2.

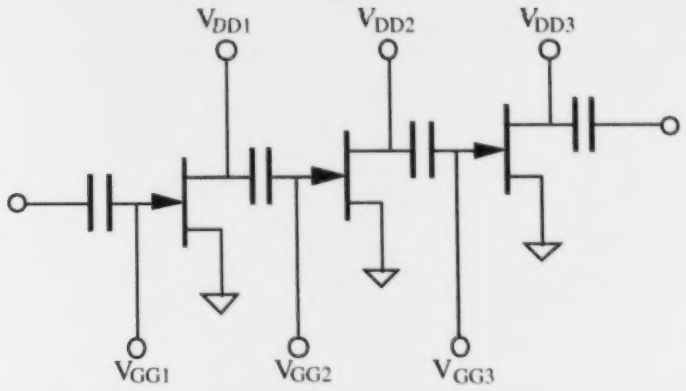


Figure 1.2 Three-stage FET amplifier, capacitively coupled

This configuration has the advantage of simplicity when compared with other configurations such as (a) a balanced amplifier, where the input signal is split into two equal parts by a Lange coupler, amplified, then recombined at the output, or (b) a novel configuration that splits the input signal into low-frequency and high-frequency bands, amplifies each band separately, then recombines them at the output. Also, the overall noise figure depends predominately on only two components: the quality of the first stage transistor and any resistive biasing component(s) at its gate.

The most difficult aspect in wideband microwave amplifier design is impedance matching between stages. The gain, which is the magnitude and phase of s_{21}, of microwave transistors such as MESFETs changes at microwave frequencies. So does the magnitude and phase of s_{11} and s_{22}, as can be seen from the transistor data sheets in Appendix A. Therefore, the biasing circuits, along with special interstage impedance-matching networks, must equalize the gain and match the output impedance of a stage to the input impedance of a following stage in order to obtain a flat gain spectrum. In general, for a wideband microwave gain block connected to arbitrary source and load impedances Z_s and Z_l, we have the situation shown in Figure 1.3.

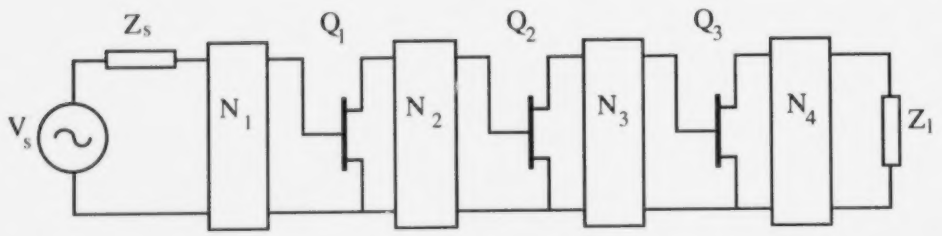


Figure 1.3 Multi-stage microwave MESFET amplifier, with interstage impedance-matching networks

The goal is to design and construct the impedance-matching networks N_1, N_2, and N_3 to match the input and output impedances of the transistor cascade to the source and load impedances Z_s and Z_l, which are typically 50 Ω, and to match the complex input impedance of any given stage to the complex output impedance of the previous stage. Also, these networks must compensate for any change in s_{21} of the transistors to meet the goal of constant gain from source to load over a prescribed bandwidth.

In order to extend the 3-dB down bandwidth at the high frequency end of this kind of amplifier, a technique called inductive peaking [2,3,4] is used. This involves placing a small inductance, typically on the order of one nanohenry, at the gate, at the drain, and/or in a drain-to-gate feedback loop, which has the effect of creating a slight increase, then a rapid decrease in gain at the point in the frequency spectrum where an unpeaked amplifier would begin to roll off. This is illustrated in Figure 1.4.

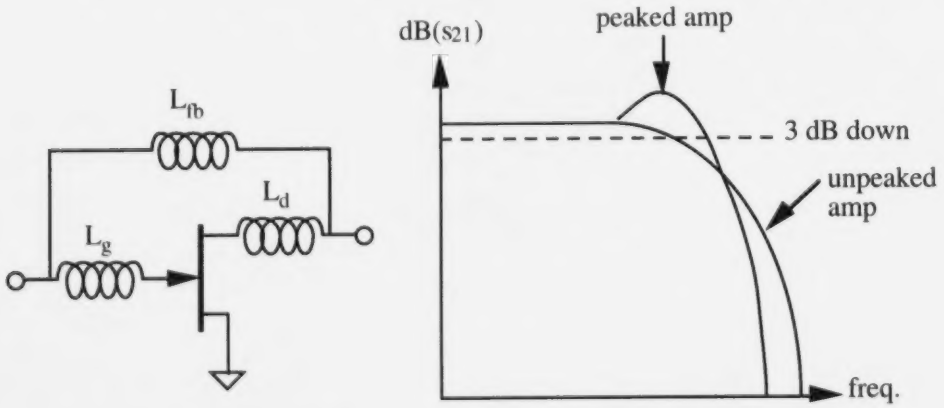


Figure 1.4 Circuit for and effects of inductive peaking

1.2 Optical Receiver Configuration and MSM Photodetectors

In order to be re-configurable as an optical receiver, a design topology for the wideband electronic amplifier must be chosen that is flexible enough to permit such a change. The major difference that must be accommodated is the change in signal source impedance. For a microwave amplifier, the standard impedance of coaxial transmission lines, signal sources, and loads is 50 Ω. For photodiodes (PDs) such as p-i-ns and avalanche photodiodes (APDs), and double Schottky junction metal-semiconductor-metal (MSM) photodetectors (PDs) such as the ones to be used in this project, the source consists of a photocurrent source and a very small capacitance, typically a few tenths of a picofarad, formed by the metal contacts and semiconductor dielectric of these devices. The structure of an MSM PD and its circuit symbol is shown in Figure 1.5.

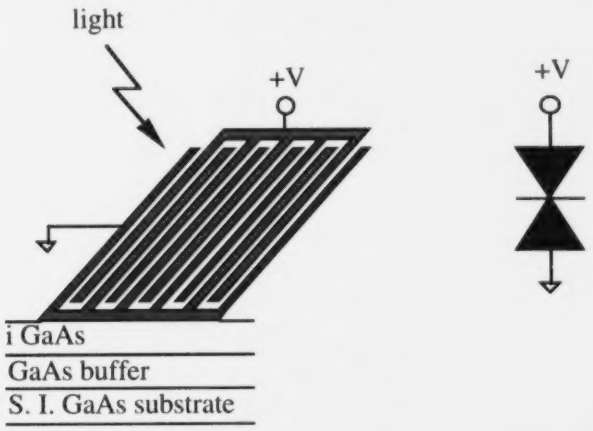


Figure 1.5 Simple MSM structure and circuit symbol

1.3 Organization of the Thesis

Chapter 2 will discuss the various topologies and components used in the amplifier and optical receiver. Chapter 3 will present the reasons for the design choices made, and give detail on the actual design and circuit simulations, which were carried out using Hewlett-Packard's Microwave Design System (MDS), as well as construction details. Chapter 4 contains all experimental results, and chapter 5 provides discussion of the results and conclusions.

2. Device and Design Considerations

The overall design objective for the electronic amplifier is 20 dB of gain from a few MHz to 6 GHz. Gain over this frequency range must be as flat as possible, preferably with ripple less than 1 dB, in order that there be little or no ISI for 10 Gbit/s signals. Also, a low noise figure and good input and output impedance matching to 50 Ω is required.

2.1 Active Device Theory of Operation: The MESFET

As stated in Chapter 1, GaAs MESFETs are chosen instead of HBTs as the active devices in wideband hybrid MIC amplifiers for multigigabit per second systems. The rudimentary construction of a typical small-signal, n-channel microwave GaAs MESFET is depicted in Figure 2.1.

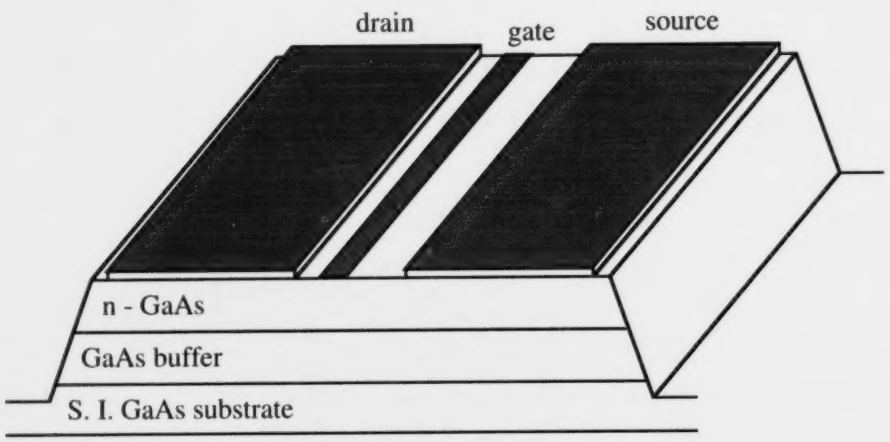


Figure 2.1 Microwave GaAs MESFET structure

On top of a highly resistive semi-insulating (S. I.) GaAs substrate, a buffer layer of GaAs is grown to isolate the MESFET structure from the substrate and any other potential near-by structures. An n-doped GaAs channel is then deposited, and on top of that are the drain, gate, and source contacts. Typically layers of titanium, tungsten, and gold, the drain and source are ohmic contacts, sitting on a thin layer of highly n-doped GaAs, while the gate and channel form a Schottky, or metal-semiconductor, junction. The area around the device is then etched away to the substrate, thus forming an isolating mesa. For small-signal MESFETs, typical gate length is less than 1 μm, usually around 0.3 μm, and typical gate widths are a few hundred μm, usually about 300 μm.

This depletion-type FET operates in a straightforward way. In a common source configuration as depicted in Figure 1.1, DC bias current flows through the channel from the drain to the source, typically a few tens of mA. The voltage drop across the channel is usually between two and four volts. The gate-source junction is reverse biased by a few tenths of a volt to create a depletion region in the channel just under the gate. Finally, a small AC input voltage applied across the gate-source junction modulates the size of the depleted region below the gate, thus modulating channel current. Output voltage appears at the drain.

By using GaAs instead of silicon, much higher electron mobility in the channel is achieved. Therefore this device can operate well at higher frequencies. There is no diffusion involved in the manufacturing, so gate lengths can be made very short, leading to low gate-source capacitance (C_{gs}), making this device even more suitable for high frequency operation. The transconductance, g_m, defined as AC drain-source current divided by AC gate-source voltage (i_{ds}/v_{gs}) of MESFETs is high, typically 30 mS to more than 50 mS.

2.2 HEMT Structure and Operation

A HEMT is an improved version of a GaAs MESFET. Increasing channel conductivity, which leads to increased transconductance and lower noise, can be accomplished by increasing the doping in the n-type channel, which increases carrier concentration, carriers being electrons. However, this increased doping leads to increased scattering off the added impurities. The net effect is to lower electron mobility. In order to create a high electron concentration in the channel by means other than doping, a type of "band-gap engineering" is done using III-V semiconductor compounds called modulation doping. This is accomplished by growing a thin undoped "well" of GaAs bound by a wider band gap, doped "barrier" of AlGaAs, as shown in Figures 2.2a and 2.2b.

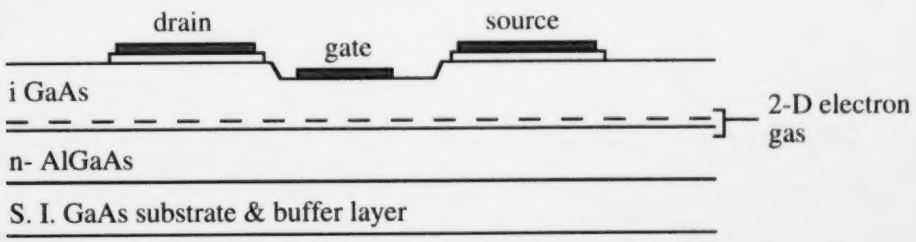


Figure 2.2a Simple HEMT layer structure

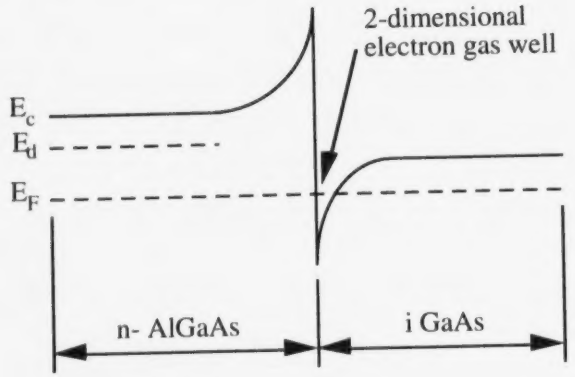


Figure 2.2b HEMT conduction band diagram

Electrons from the n-doped AlGaAs layer fall into the potential well and become trapped, creating a very thin, almost two-dimensional electron gas layer in the channel. The donor atoms remain in the AlGaAs, creating an undoped GaAs layer filled with free electrons. Electron mobility is approximately that of bulk GaAs with no impurities. This effect can be even stronger at low temperatures, where lattice or phonon scattering is also low. Electron mobility is greater than 250 000 cm^2/Vs at 77°K, and greater than 2 000 000 cm^2/Vs at 4°K.

HEMTs are also known by other names, usually MODFETs (modulation-doped FETs), but also as 2-DEGFETs or TEGFETs (two-dimensional electron gas FETs), or even SEDFETs (separately-doped FETs).

2.3 Electrical Characteristics of MESFETs and HEMTs

MESFET and HEMT chips are available from several manufacturers, such as Hewlett-Packard and NEC. The HEMTs used in this project were Fujitsu models FHX 04X and FHX 06X. The transistor data sheets supplied in the manufacturer's catalog and the data sheets sent along with the devices are given in Appendix A.

There is considerable information on these data sheets. First, typical FET DC parameters are supplied. Maximum drain-source current I_{DSS}, pinch-off voltage V_p, gate-source breakdown voltage V_{GS0}, transconductance g_m, and I_{DS} vs. V_{DS} curves are presented. Typical small-signal s-parameters are given with the HEMT in a common source configuration and at one bias point only, I_{DS} = 10 mA and V_{DS} = 2 V. The gate and source form port one, while the drain and source form port two. Note how the magnitude of s_{21} decreases and phase of s_{21} rotates as frequency increases. This is due to the input

signal appearing across the gate-source capacitance of the device, which acts as a smaller and smaller impedance as frequencies become higher and higher. The magnitudes of s_{11} and s_{22} also decrease with frequency, mainly due to the internal capacitances C_{gs} and C_{ds}. The physical dimensions of the chip are given. Gate width is approximately 300 μm. From the size and position of the gate, drain, and source pads, it is possible to determine how the prescribed bond wires that connect the HEMT to the rest of the circuit are to be made. The measured s-parameters include the inductive effects of the bond wires, allowing circuit designers to use the s-parameters of the device as it actually will appear in a real circuit. Typical noise parameters such as Γ_{opt}, the optimum source reflection coefficient, NF_{min}, the minimum achievable noise figure, and R_n, the equivalent noise resistance, are included. These are the standard noise characteristic parameters [5] of a two-port device, and are explained in the next paragraph.

Consider a general noisy two-port network connected to a source with an arbitrary, known admittance Y_s and a load Y_l in a system with characteristic impedance Z_0 as in Figure 2.3.

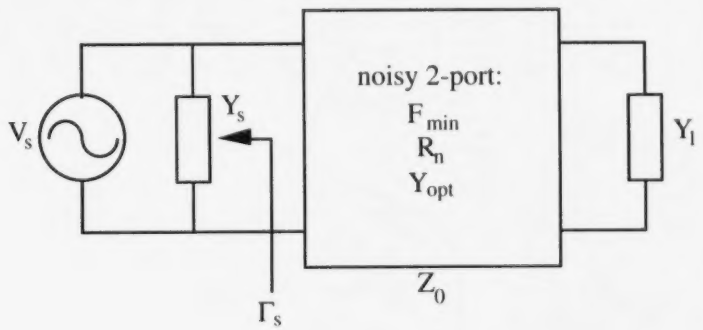


Figure 2.3 Noisy 2-port network connected to source and load

The noise figure, F, of this amplifier is then given as

$$F = F_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{opt}\right|^2$$

where $Y_s = G_s + jB_s$ is the source admittance presented to the network, Y_{opt} is optimum source admittance which results in the network exhibiting its minimum possible noise figure, F_{min} is the minimum noise figure of the network, attained when $Y_s = Y_{opt}$, R_n is the equivalent noise resistance of the network, and G_s is the real part of Y_s.

Alternatively, if Γ_{opt}, the optimum source reflection coefficient for minimum noise figure, is specified instead of Y_{opt}, then noise figure is given by

$$F = F_{min} + \frac{4R_n}{Z_0} \frac{\left|\Gamma_s - \Gamma_{opt}\right|^2}{\left(1 - \left|\Gamma_s\right|^2\right)\left|1 + \Gamma_{opt}\right|^2}.$$

Γs is the reflection coefficient seen by the noisy 2-port looking towards the source.

Note how F approaches F_{min} as Y_s nears Y_{opt}, or Γ_s nears Γ_{opt}. These equations describe how noise figure grows as source impedance deviates from ideal source impedance. The Fujitsu FHX transistors are all manufactured together using the same processing, then sorted into three models based on their noise figure as measured at the factory.

Finally, even though this transistor is intended for small-signal applications, output power can be on the order of 10 dBm in the linear gain regime.

2.4 Small-Signal Equivalent Circuit Modeling

In order to use the transistor data sheet information in circuit simulations, the two-port s- and noise parameter data of the FHX 04X HEMT was entered into a generic s-parameter component in Hewlett-Packard's (HP's) Microwave Design System (MDS). In fact, HP includes this data in a Fujitsu MESFET small-signal library, which was available. The information was five years old, and there were slight differences in the noise data between the library and the data sheets, so a new s-parameter model including the noise parameters from the data sheet was created.

Using the measured s- and noise parameter data, it was possible to construct a small-signal equivalent circuit model of the FHX 04X HEMT. The component values of a well-known MESFET equivalent circuit shown in Figure 2.4 were adjusted until its s-parameter values matched the measured s-parameters from the data sheets. This approach provided insight into the operation of the device and some of the more important modeling components that are not obvious from the measured s-parameter data, such as internal capacitances C_{gs}, C_{ds}, and C_{gd}, also inductance values L_g, L_d, and L_s. This modeling was done using MDS, and the resulting equivalent circuit model reproduced the measured s-parameters exactly from 100 MHz to 22 GHz, which is the frequency range for which s-parameters are given on the manufacturer's data sheets.

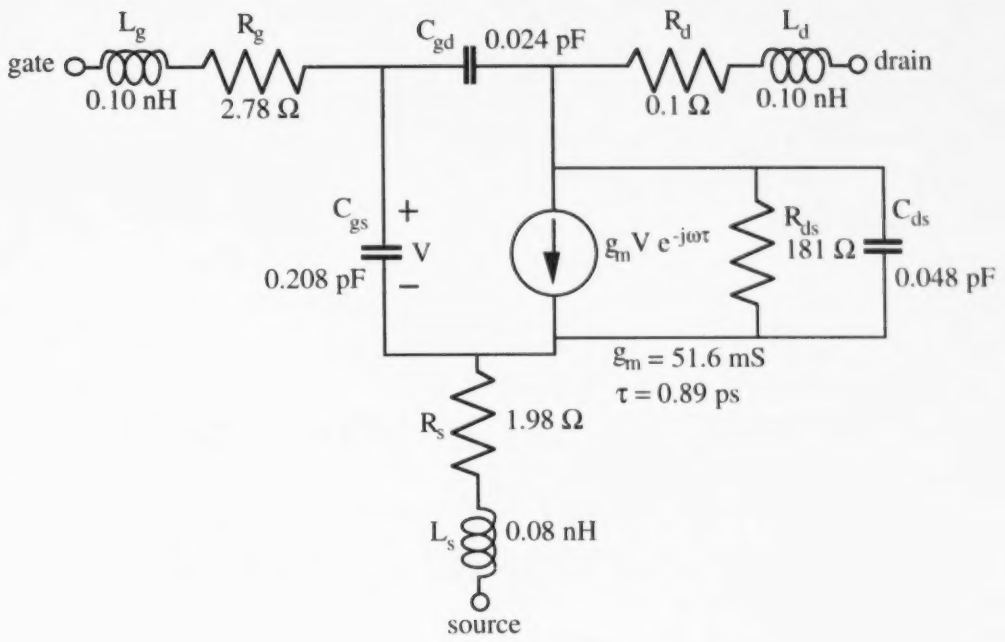


Figure 2.4 FHX 04X/05X/06X small signal equivalent circuit

2.5 GaAs Metal-Semiconductor-Metal (MSM) Photodetectors

As mentioned briefly in Chapter 1, the photodetectors to be used in this project when the electronic amplifier is re-configured as an optical receiver are GaAs metal-semiconductor-metal (MSM) devices. The structure of MSMs is depicted in Figure 2.5. In brief, their construction and operation principles are as follows.

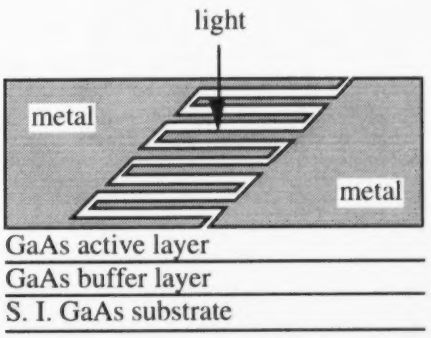


Figure 2.5 GaAs MSM structure

An epitaxially-grown buffer layer of GaAs is deposited on top of a semi-insulating GaAs substrate to confine the MSM. Then, an intrinsic layer of GaAs, typically about 1 μm thick, is grown on top of the buffer layer. Finally, thin, interdigital metal fingers, usually layers of titanium, tungsten and gold, are laid down in the pattern depicted in Figure 2.5. Typical finger width and space between fingers is on the order of a few μm. The area immediately surrounding the MSM structure is etched down to the substrate, isolating the MSM region on a mesa, thus preventing photogenerated charge carriers in the active layer from migrating away from it. These processing steps are very much like those involved in the fabrication of MESFETs and HEMTs, which has led many people to attempt simultaneous monolithic integration of MSM and MESFET or HEMT devices to create monolithically integrated, very wide band optical receivers. References [6] and [7] are two examples of these monolithic optical receivers.

When a bias voltage is applied across the two sets of interleaved fingers of an MSM, an electric field is formed in the GaAs active layer beneath the fingers. When 800-nm wavelength light strikes the top of the MSM, some is reflected by the fingers, and the rest enters the GaAs active layer, creating electron-hole pairs which are then very quickly swept to the fingers of the MSM by the electric field. MSM PDs are well suited for very high speed photodetection due to the very low capacitance between the metal fingers. Typical MSMs with areas of about 100 μm by 100 μm and 1 μm finger spacing and finger width can have an internal capacitance of tens to a hundred or so fF.

The GaAs MSMs used in this project were arranged in 1 by 8 linear arrays. The GaAs MSM array chip, made by Bell-Northern Research (BNR), contains eight 100 μm by 100 μm MSMs with 1 μm wide fingers and 3 μm between adjacent fingers, spaced 250 μm apart with one common bond pad joining one terminal of each of the MSMs together. These arrays were fabricated for potential use in very high speed optoelectronic switching or signal processing [8]. The physical layout of these MSM arrays is depicted in Figure 2.6 below.

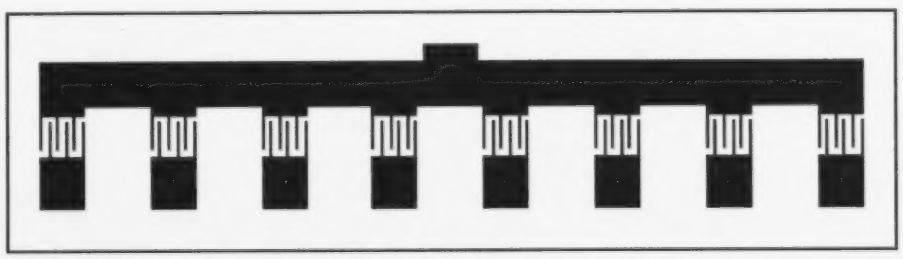


Figure 2.6 BNR's 1 by 8 GaAs MSM arrays

2.6 The History of Wideband Microwave Amplifier Design

2.6.1 "Real Frequency" Broadband Multistage Microwave Matching

In the early-to-mid 1970s, GaAs MESFETs were invented, and became the subject of intense study for use in high-speed and microwave applications. In the late 1970s and early 1980s, H. J. Carlin developed a way of designing lossless, equalizing two-port networks that could be placed between FETs in an amplifier consisting of a cascade of FETs in order to match input and output impedances and equalize overall gain over a wide bandwidth, thus forming broad-band, high-gain microwave amplifiers [9,10]. The general circuit topology appears in Figure 2.7.

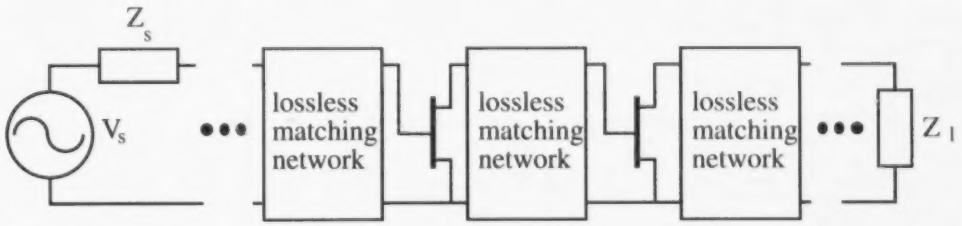


Figure 2.7 General multi-stage wideband microwave amplifier with lossless interstage matching networks

This circuit is an example of what is known as the double-matching problem. The first match involves transferring power from a complex generator to the input of an equalizer, and the second match is from the equalizer to an arbitrary load. Conceptually, the matching procedure is as follows.

Start with an arbitrary but known source impedance, arbitrary but known load impedance, and a two-port equalizer E in between consisting of a network of ideal inductances and capacitances. The s-parameters of this equalizer can be expressed in terms of polynomials $g(s) = g_0 + g_1 s + g_2 s^2 + ... + g_n s^n$ and $h(s) = h_0 + h_1 s + h_2 s^2 + ... + h_n s^n$. Denoting e_{ij} rather than s_{ij} $\{i, j = 1,2\}$ as scattering parameters for the equalizer yields: $e_{11}(s) = h(s)/g(s)$, $e_{21}(s) = s^k/g(s)$, $e_{12}(s) = -s^k/g(s)$, and $e_{22}(s) = -(-1)^k h(-s)/g(s)$, where n is the number of lumped inductive and capacitive components in E and k is the degree of the numerator polynomial of $e_{21}(s)$. In order to determine the coefficients of the polynomials h(s) and g(s), start by specifying a fixed number of components in E, which fixes n and k, and guess at values for the coefficients of h(s). Using the frequency-

dependent reflection coefficients of the source and load attached to the equalizer E, Carlin [9,10] provided a procedure for generating the coefficients of g(s) and h(s) that produce a constant transducer power gain through the equalizer E over a specified bandwidth. Each matching network in the cascade can be designed one at a time using this technique.

Carlin produced good wideband designs with this procedure from very simple matching networks that consisted of one series inductance and one shunt capacitance. The major drawbacks of his work were that this procedure required a great deal of complicated computer programming. Also, he made no attempt to construct any of the circuits given in [9] and [10]. Still, this work was carried out without the aid of microwave circuit simulation software, and stands as a pioneering effort in interstage matching network design for wideband microwave amplifiers.

2.6.2 Interstage Matching Using Distributed Components

In 1981, Honjo and Takajama [11] produced a design and realization of an ultra-broad band GaAs FET-based amplifier, suitable for multi-Gbit/s data rate systems. They started by comparing frequency-gain characteristics of four different types of wideband, high frequency amplifiers based on GaAs MESFETs, their relative merits, and inherent drawbacks. This is summarized below.

(i) Conventional RC coupled amplifiers
  pros: high, flat gain, all the way down to low MHz frequencies
  cons: small 3 dB-down bandwidth

(ii) Negative feedback amplifiers
  pros: wider bandwidth than RC coupled amplifiers
  cons: lower gain than RC coupled amplifiers, added design difficulty for impedance matching, potential stability problems, excess noise contributed by resistive feedback components

(iii) (Inductive) peaking amplifiers
  pros: slightly higher high-frequency roll-off than RC coupled amps
  cons: gain ripple

(iv) Conventional wideband microwave amplifiers
  pros: has gain at frequencies higher than other amplifiers
  cons: has no gain at frequencies below microwave region, interstage impedance matching using transmission lines is limited by physical size considerations

The gain spectra of these four types of wideband amplifiers are graphically summarized in Figure 2.8.

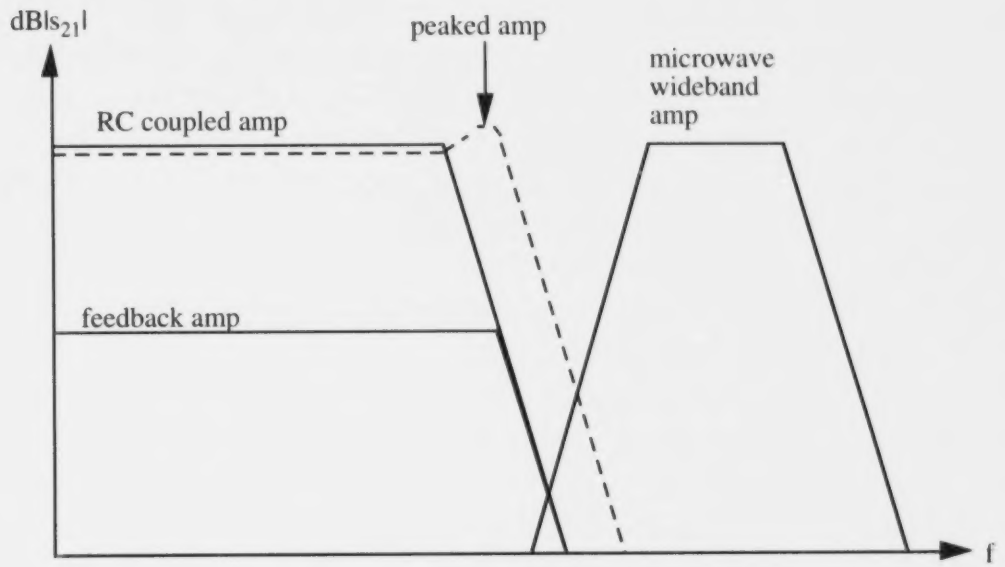


Figure 2.8 Gain profiles of four types of wideband amplifiers

Honjo concluded that the way to make an "ultra-broad-band" amplifier was through a combination of the first and last types of amplifiers. The favorable low-frequency characteristics of the conventional RC coupled amplifier can be combined with the favorable high-frequency characteristics of the traditional microwave wideband amplifier to achieve flat gain from several MHz to multiple GHz. The circuit topology is shown in Figure 2.9, with coupling capacitors and biasing neglected for clarity.

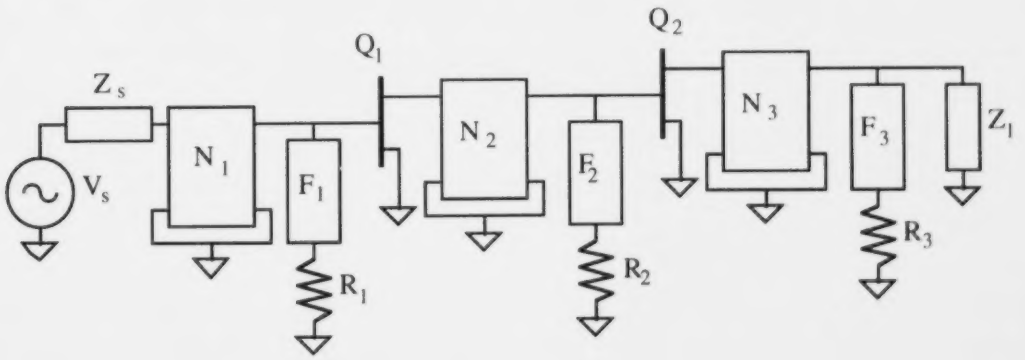


Figure 2.9 Combining topologies to make an "ultrabroadband" amplifier

The design of the lossless, high-frequency impedance-matching networks N_1, N_2, and N_3, which were made from microstrip transmission lines and transmission line stubs of various characteristic impedances and lengths, and the impedance transforming components F_1, F_2, and F_3 was done using a computer circuit simulator. The circuit was constructed on a 25-mil thick alumina ceramic substrate, and the metal traces were gold on chrome. Thin film resistors were made from Ta_2N and capacitors were multilayer, high-dielectric-constant ceramic.

To realize a two-stage amplifier with general interstage matching and transforming components, Honjo and Takajama [11] designed and built two amplifiers. Model A was to have 10 dB of gain and a 3 dB-down bandwidth of 10.5 GHz, while model B was to have 15 dB of gain up to 7 GHz. After construction, these two amplifiers very nearly met these design objectives, with 8.6 dB of gain up to 9.5 GHz for model A and 14 dB of gain up to 6 GHz for model B. For model A, other notable characteristics include more than 10 dBm of output power before gain begins to fall, input standing wave ratio (SWR) of 4 or less, output SWR of less than 2, and noise figure between 8 and 10 dB.

This work shows the benefits of interstage matching techniques using distributed microstrip transmission line components. The only potential drawback of designing and fabricating a wideband amplifier in this way is that there is very little if any room for fine tuning the distributed interstage matching components after they have been fabricated.

2.6.3 TFB-Based Wideband Amplifier Design

The next development in very wideband microwave amplifiers for Gbit/s signals comes from Perennec et al. [12,13] in 1989. They dealt with the deficiencies of Carlin's work, namely not enough bandwidth down to the low MHz region and no physical realization. Also, Perennec aimed to achieve more gain than Honjo, and lower input and output SWRs. The main difference between this work and that of the other two groups was the introduction of the concept of a transistor feedback block (TFB) module to be used in place of FETs. In order to make multiple stages of GaAs MESFETs easier to match, various passive components are connected to the FET to reduce the high input impedance/reflection coefficient and to lower and flatten the gain. A TFB is shown in Figure 2.10.

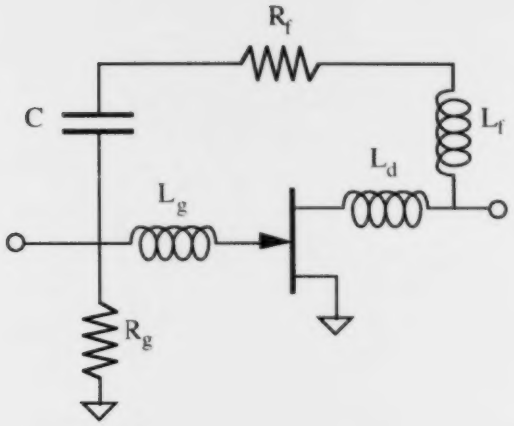


Figure 2.10 The transistor feedback block (TFB)

Perennec et al. [12,13] determined the following passive component values for a TFB circuit containing the RTC-CFX 31X GaAs FET:

- Feedback resistor $R_F = 330\ \Omega > g_m Z_0^2$
- Decoupling capacitor C = 50 pF reduces feedback at lower frequencies
- Input damping resistor $R_g = 680\ \Omega$
- Feedback inductance $L_f = 3.3$ nH reduces feedback at higher frequencies, increasing gain, and prevents oscillation
- Drain inductance L_d = about 1.5 nH or less, to compensate for transistor C_{ds}.
- Gate inductance L_g = about 1.5 nH or less, for input matching and gain at high frequencies.

Then, using TFBs in place of FETs, Perennec et al. [12,13] designed a cascaded 3-stage amplifier with lossless interstage matching networks, using the same algorithm as Carlin, but with an additional routine for keeping input and output reflections low. This design resulted in a calculated gain of 22 dB up to 6 GHz, with the matching networks consisting of ideal lumped inductors and capacitors. However, the measured gain of a hybrid realization of the design demonstrated a low-frequency gain of almost 20 dB, slowly decreasing to just under 16 dB at 20 MHz, then about 2 dB of ripple before falling off at 6 GHz. Input and output SWRs were measured to be less than 3, and noise figure was claimed to be less than 9 dB.

With so many capacitances of less than a picofarad and inductances of a few nanohenrys, and feedback, present in the amplifier design, it is not surprising that the measured results deviated strongly from the predicted response of this circuit. It must have been difficult to accurately fabricate such inductance and capacitance values for operation at

multi-GHz frequencies. Also, no doubt distributed parameter effects inside lumped circuit elements contributed to the lowered response.

2.7 Direct Detection Optical Receivers for Multi-Gbit/s Systems (Hybrid MIC construction)

Wideband microwave amplifiers such as the ones that these three research groups designed and/or built find their intended application in multi-Gbit/s lightwave systems, which require very high frequency optical to electrical conversion before signals can be electrically amplified. Thus, the closely related area of hybrid MIC wideband optical receiver design is introduced here. There are three major differences between optical receivers for Gbit/s systems and electronic amplifiers for Gbit/s systems. These differences are:

- Input is no longer a 50 Ω electrical source. Rather, it is light shining on a photodetector which converts the light to a current source. Often, a p-i-n photodiode (PD) is used for Gbit/s optical receivers [14,15,16], while some receivers are made with an avalanche photodiode (APD) [17,18,19]. The output of the PD is then fed into the gate of a common-source configured GaAs MESFET or HEMT to be amplified. The circuit symbol and the typical equivalent circuit of photodiodes used in the design of optical receivers is shown in Figure 2.11.

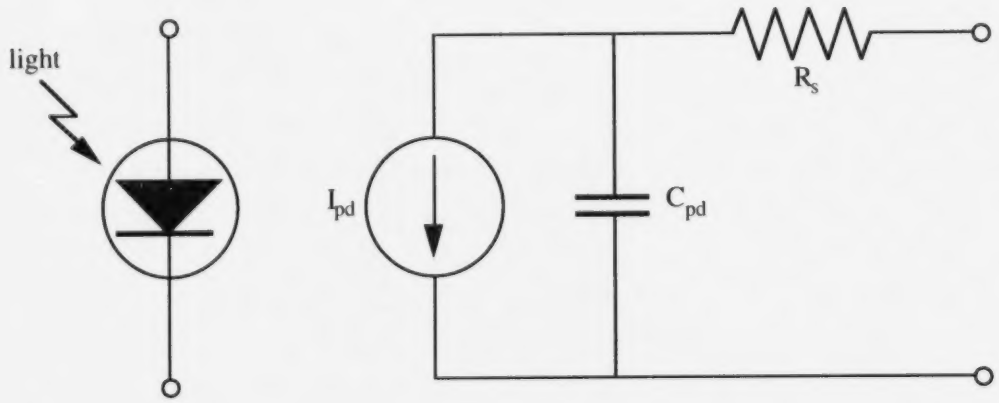


Figure 2.11 Photodiode circuit symbol and equivalent circuit

- Noise performance is no longer expressed as noise figure, but rather as equivalent input r.m.s. noise current spectral density, which is the equivalent noise current spectral

density which would have to appear across I_{pd} in the above equivalent circuit model of a PD to generate the noise spectrum seen at the output of the receiver.

- Gain is no longer the magnitude of s_{21}. Rather it is transimpedance, due to the fact that the input is now a current source, and output is voltage, making the gain equal to output voltage divided by input current, or impedance. Generally, this transimpedance is expressed as dBΩ, defined as $20\log_{10}(|\text{transimpedance}|)$.

2.7.1 Optical Receivers and Interstage Matching

James L. Gimlett [20,21] designed and built multi-stage Gbit/s optical receivers using the same kind of distributed component interstage matching that Honjo and Takajama [11] used in their electronic amplifiers. Using resistive and lossless transmission line components to bridge the gap between low RF frequencies and microwaves, and a commercially-available InGaAs p-i-n PD suitable for receiving 1.3 μm wavelength light at the input, Gimlett succeeded in producing an optical receiver using the basic topology shown in Figure 2.12. L_1 is the inductance of the bond wire joining the PD to the amplifier input, and again biasing and coupling are omitted.

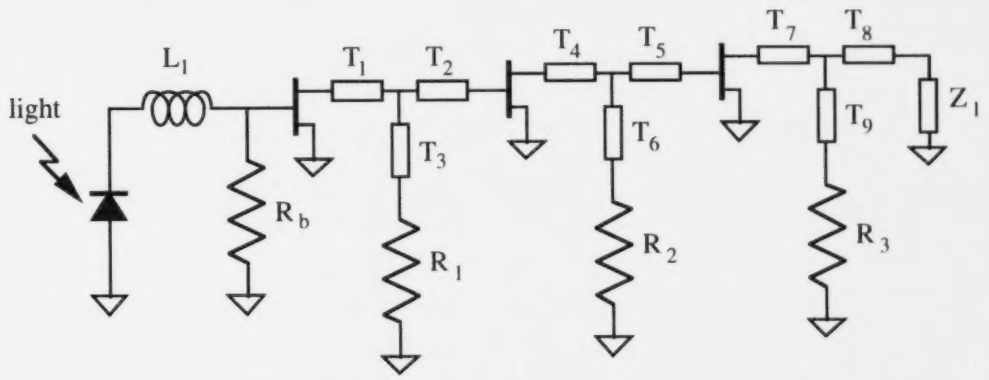


Figure 2.12 Gimlett's 8 GHz optical receiver topology

The impedance and length of the nine transmission line elements T_1 to T_9 were optimized to achieve flat gain up to 8 GHz with the aid of the microwave circuit simulation program TOUCHSTONE. The circuit was then constructed as a thin-film hybrid MIC, using NEC 71000 GaAs FETs. Each of the first two stages were to generate about 10 dB of gain, while the third stage provided an impedance match to a 50 Ω load. Bandwidth was 50 kHz to more than 8 GHz, and equivalent input noise was less than 7 pA/√Hz in the passband. Overall, this is a notable advance in the state of the art.

2.7.2 Inductive Peaking Techniques

There is one more design technique to consider: inductive peaking, which was touched on briefly in the first chapter. Based on calculations and simulations, Ohkawa [2] showed that four different inductive peaking topologies increase 3 dB-down bandwidth over a simple shunt feedback case. For a given FET, feedback resistor R_f, feedback capacitor C_f, and optimized peaking inductor values, each of the amplifier stages shown in Figure 2.13 was designed as the first stage of a two-stage optical receiver, and the corresponding overall calculated bandwidth of the receiver is shown for each case.

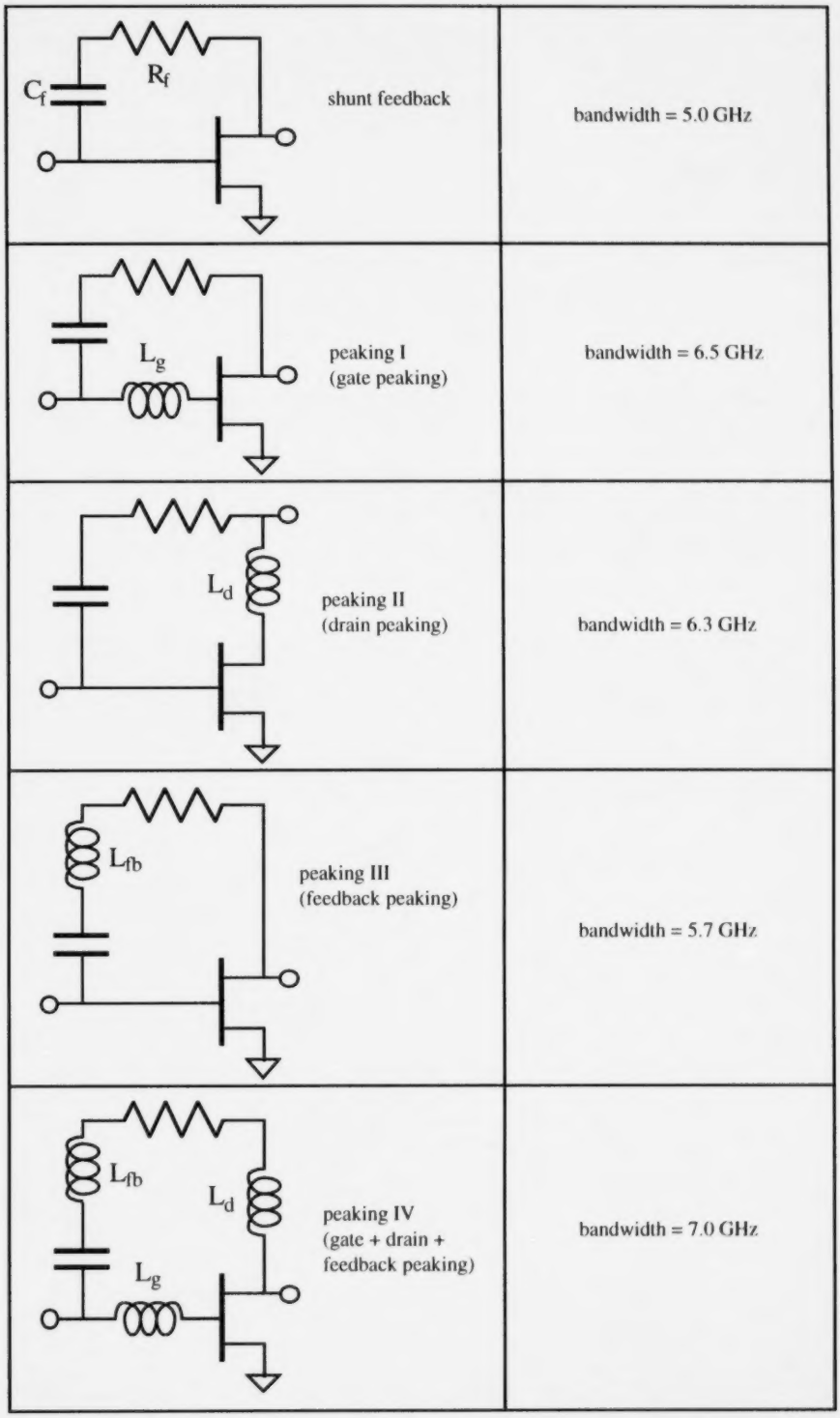


Figure 2.13 Inductive peaking topologies and associated bandwidths

Using this information, Ohkawa constructed a three-stage optical preamplifier without complicated interstage matching networks to equalize gain, but rather with feedback, and gate and drain inductive peaking, shown in Figure 2.14. Each stage develops about 7 dB of gain.

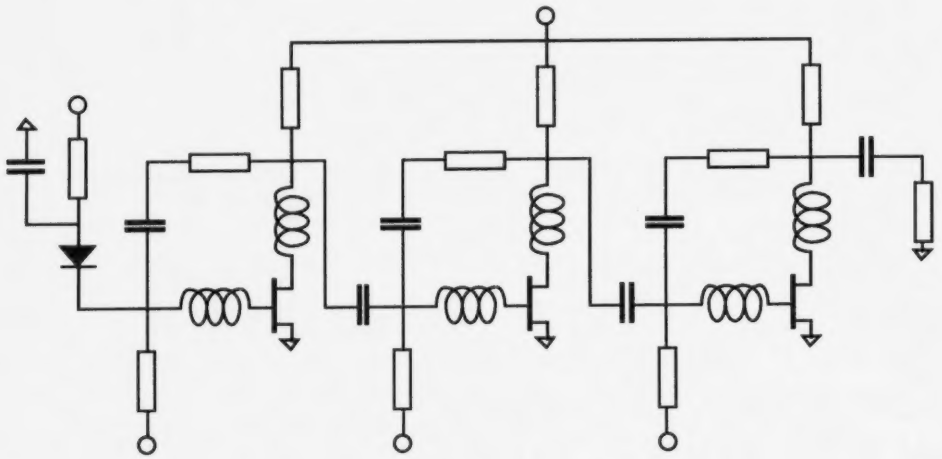


Figure 2.14 3-stage optical preamplifier, using feedback and inductive peaking

This circuit was constructed from HEMTs and resistor chips on a quartz substrate, and presumably chip capacitors and bond wires for inductances. Circuit component values were optimized using the microwave circuit simulation software TSPICE. Measured 3 dB-down bandwidth was 20 GHz, with nominal passband gain of 21.5 dB, with little ripple, and transimpedance of 58 dBΩ with less than 3 dB of ripple. The measured noise figure was 4 dB, and equivalent input noise was 7.6 pA/√Hz. This was a major achievement.

The work described in this thesis is the result of the author applying the best and/or most appropriate features of each of these four authors' achievements.

3. Design and Construction

3.1 Guiding Ideas

There were two objectives in the design process. One was the desire to make the final product easy to trim. It is difficult to anticipate all significant sources of impairment at gigahertz frequencies and over a wide bandwidth, so it was virtually certain that it would be necessary to empirically adjust component values to produce desired results. This meant that circuit topology would have to be relatively simple. This led to the second objective of avoiding any kind of feedback arrangement.

It was decided, as stated earlier, to use three stages of common-source-configured HEMTs. From [22], a common source configuration results in the first stage having high short-circuit current gain and high output impedance, the two conditions that minimize noise contributions of any subsequent stages to overall amplifier noise performance. Three stages were chosen to provide the required level of gain.

Interstage impedance matching was not based on lumped inductor and capacitor components, as postulated by Carlin [9,10] and fabricated by Perennec et al. [12,13], because of the difficulty involved in accurately fabricating adequate inductance values from gold wire bonds using a manual wire bonder and the cost, time, and/or complexity of purchasing or fabricating adequate capacitance values, which would be about 1 pF or less. Furthermore, several of each of these special components would have to be made in order to realize just one amplifier. The distributed transmission line and stub matching circuits of Honjo and Takajama [11] were rejected as well, because of the difficulty of altering their size to realize the designed response.

Also, it was not possible to rely absolutely on the published typical g_m, I_{DSS}, V_p, or measured s- and noise parameters of the FHX 04X/06X HEMTs being used. Comparing the transistor data from the Fujitsu catalog and the specification sheets sent with the devices confirms this. The overall design had to be flexible in part because of the variability of the active devices.

Honjo and Takajama [11] were very correct when they wrote that negative feedback topologies would complicate impedance matching between stages. Along with any impedance associated with feedback components would be phase shift due to transmission line effects in the feedback path, making circuit design very complicated. This became abundantly clear during circuit simulations. As stated in Chapter 2, other potential problems associated with feedback include lower gain, added noise, and the possibility of oscillation.

Inductive peaking appeared to be a very attractive design option, and so was included in the design. It was decided to use only gate peaking at each stage. This was due to the desire to avoid any kind of feedback, and the fact that gate peaking is slightly more effective than drain peaking [2]. Again, the difficulty associated with forming more than a few accurate inductances in the nanohenry range played a role in this decision.

The net effect of all these decisions led to the creation of an Ohkawa-type peaked amplifier with gate peaking and no feedback, rather than a Carlin or Perennec-type amplifier with complicated interstage matching networks that would have a significant potential to not function well in the event that the lumped or distributed components of these networks were not accurately made or had significant unaccounted-for parasitic effects.

Using simple mid-band, low-frequency, and high-frequency equivalent circuits and transistor amplifier theory, it can be shown that the potential exists for this amplifier topology to meet the goals of this project. Starting with the proposed three-stage FET amplifier as shown in Figure 3.1, a mid-band equivalent circuit is developed as shown in Figure 3.2.

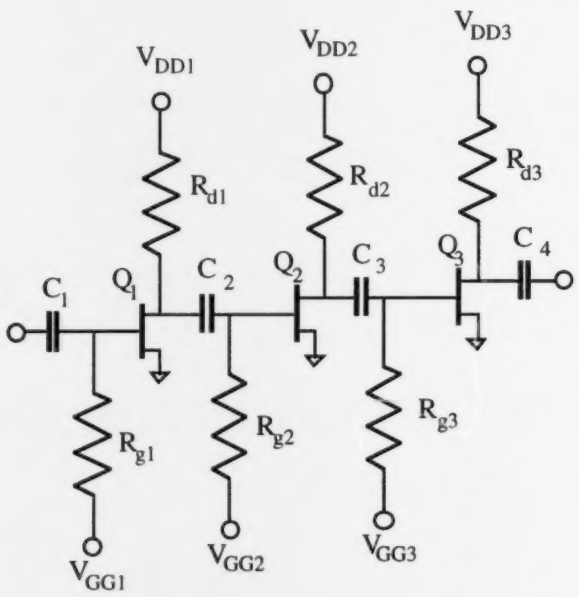


Figure 3.1 Basic three-stage FET amplifier

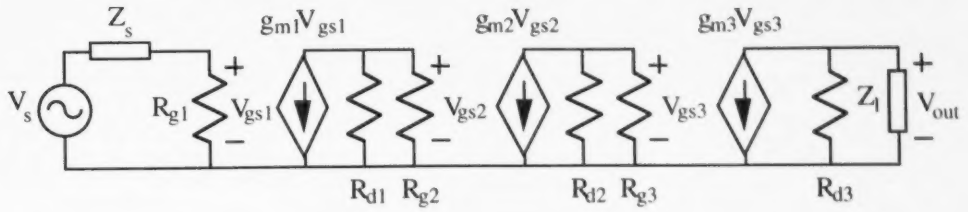


Figure 3.2 Midband equivalent circuit of three-stage amplifier

The gain in the passband of the amplifier, A_{v0}, is the gain of the amplifier for the frequency range where all coupling capacitors are essentially short circuits and capacitances within the transistors are essentially open circuits. A_{v0} is a function of bias resistors and FET transconductances, and is given by

$$A_{v0} = \frac{V_{out}}{V_s} = g_{m1}g_{m2}g_{m3}\left(\frac{R_{g1}}{R_{g1}+Z_s}\right)\left(R_{d1}\|R_{g2}\right)\left(R_{d2}\|R_{g3}\right)\left(R_{d3}\|Z_l\right),$$

where the parallel vertical lines || represent the parallel combination of the two impedance values on either side of the lines.

The low frequency 3 dB-down point must be a few MHz at the most. For the low frequency input stage equivalent circuit shown in Figure 3.3, low frequency gain as a function of angular frequency ω, $A_{vL}(j\omega)$, is given by

$$A_{vL}(j\omega) = \frac{A_{v0}}{1+\frac{\omega_L}{j\omega}}, \text{ where } \omega_L = \frac{1}{C_{in}\left(R_{g1}+Z_s\right)} \text{ and } A_{v0} = -g_m R_{d1}\left(\frac{R_{g1}}{R_{g1}+Z_s}\right).$$

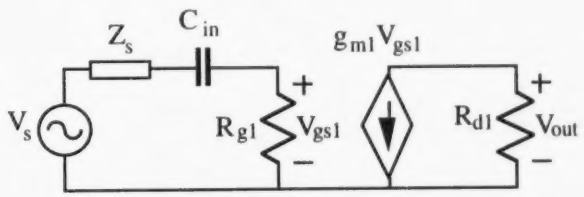


Figure 3.3 Low-frequency equivalent circuit of input stage

For a typical R_{g1} of 200 Ω, Z_s of 50 Ω, and coupling capacitor of 1.0 nF, ω_L = 637 kHz, which meets the low frequency criterion. For multiple stages, more low frequency break points are defined by coupling capacitors and the gate and drain bias resistors connected from the terminals of these capacitors to ground just as Z_s and R_{g1} provide a path to ground for C_{in} in Figure 3.3. For typical gate and drain resistor values of a few

hundred ohms, these additional low frequency roll-offs are at lower frequencies than the one defined by the input stage.

By using the internal capacitances of the FHX 04X/06X HEMT determined by the small-signal equivalent circuit modeling presented in section 2.4, an analysis of the high-frequency characteristics of the amplifier can be performed. Recall that the internal capacitances are C_{gs} = 0.208 pF, C_{gd} = 0.024 pF, and C_{ds} = 0.048 pF. By using a Miller transformation on C_{gd}, which acts as a feedback element inside the transistor itself, equivalent total input and output capacitances can be determined. Based on the high-frequency equivalent circuit of the input stage shown in Figure 3.4, the upper 3 dB-down frequency can be estimated.

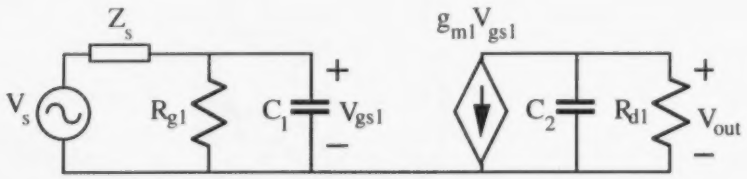


Figure 3.4 Input stage high frequency equivalent circuit

The capacitance C_1 is the sum of C_{gs} and $C_{m1} = C_{gd}(1\text{-}A)$, where A is the midband gain of the FET amplifier stage and is equal to $-g_{m1}R_{d1}$. Capacitance C_2 is the sum of C_{ds} and $C_{m2} = C_{gd}[-A/(1\text{-}A)]$. Because C_{gd} and C_{ds} are much smaller than C_{gs} and gain A will be greater than one, C_2 will be negligible compared to C_1, making the break frequency due to C_2 much higher than the high frequency roll-off caused by C_1. In much the same way as the expression for mid-band gain is altered by the addition of a factor to account for low frequency effects of coupling capacitors and resistances connected between them and ground, so too is mid-band gain altered by an additional factor to account for high frequency effects brought about by equivalent FET internal capacitances and resistances connected across them. High-frequency gain of the input amplifier stage is expressed as

$$A_{vH}(j\omega) = \frac{A_{v0}}{1 + \dfrac{j\omega}{\omega_H}}, \text{ where } \omega_H = \frac{1}{C_1\left(Z_s \| R_{g1}\right)} \text{ and } A_{v0} = -g_m R_{d1}\left(\frac{R_{g1}}{R_{g1} + Z_s}\right),$$

For a typical R_{g1} value of 200 Ω, and Z_s = 50 Ω and C_1 of about 0.3 pF, the high frequency roll-off begins to occur at 13.3 GHz, which gives plenty of margin to meet the bandwidth requirement. For multiple stages, more high frequency break points are defined by the C_1 values of each of the other FETs in the cascade and the gate and drain bias resistors connected across them, just as Z_s and R_{g1} are connected across C_1 in Figure 3.4.

For typical gate and drain resistor values of a few hundred ohms, these additional high frequency roll-offs are at even higher frequencies than the one defined by the input stage.

The amplifier was designed to resemble a low-frequency multistage amplifier. Due to the very low input and output capacitances of the HEMT chips, it was possible to use this approach to ensure low-frequency performance, yet still have gain up to several GHz. At the input, output, and between each stage, there are 1 nF coupling capacitors, gate and drain bias resistors of various values, and 1 pF "tuning" capacitors, connected from the bias resistors to ground on the resistor side away from the HEMTs. All of these components are 0805-sized chips, and all connections are made by 50 Ω microstrip traces on a 640-μm thick alumina substrate. The width of the gold-on-chrome 50 Ω microstrip lines is 624 μm, which was calculated using $\varepsilon_r = 9.8$ for alumina. At the gate of each transistor is a 125-μm-long pad on which 1.25 mil-diameter, 99.99% gold bond wire pairs of various lengths were put to form the gate peaking inductors, leaving the carefully-placed bond wires to the HEMT chips themselves undisturbed in the event of changing any gate peaking inductance.

Each source pad, one on each side of the HEMT chips, is grounded through a pair of 300-μm long bond wires to a pad on the substrate containing 200-μm diameter plated-through via holes to the chrome-gold ground plane on the bottom of the substrate. One typical stage of this amplifier appears in Figure 3.5. Plated-through via holes for tuning capacitor grounding are 400 μm in diameter.

The supplier of the chip capacitor kit used for this project, Philips, lists a +/- 0.25 pF tolerance for capacitor values from 0.47 to 6.8 pF. The chip resistors have a tolerance of 5%. Appendix B contains a detailed explanation of how bond wire lengths can be controlled to form known inductance values.

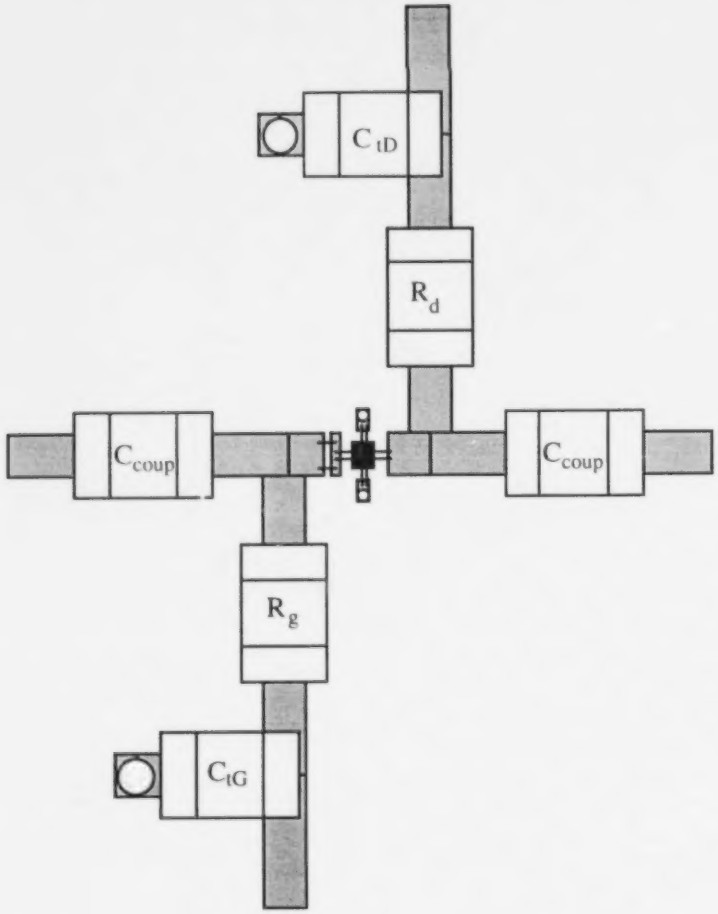


Figure 3.5 Sample layout of one stage of the amplifier

In the event that actual circuit performance differs from the design, changing C_t, R_d, and R_g values can provide a wide range of interstage frequency responses that can produce the desired result.

3.2 Circuit Simulation and Optimization

Hewlett Packard's Microwave Design System (MDS) is the microwave circuit simulator that was used in the design of the electronic amplifier and the optical receiver. MDS can also be used to generate complete layouts, graphics files that can be read by mask-making equipment, and complete documentation. Figure 3.6 is a simplified circuit

diagram of the amplifier. All "ideal wire" connections are actually 50 Ω microstrip lines, and all grounds are via holes of the sizes described earlier.

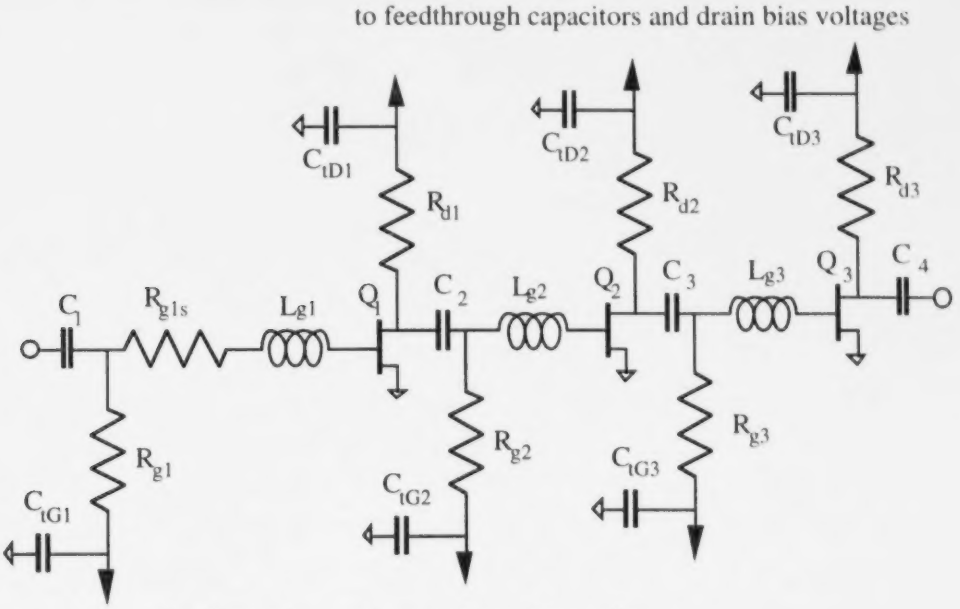


Figure 3.6 Simplified circuit diagram of electronic amplifier, as designed

Coupling capacitances C_1, C_2, C_3, and C_4 are all 1.0 nF, L_{g1}, L_{g2}, and L_{g3} are gate peaking inductors, all R_g and R_d components are gate and drain bias resistors, and R_{g1s} provides damping for large, unwanted peaking that occurred in the simulations at about 5 GHz, probably due to source-to-ground inductance. The six capacitors C_t also provide some high frequency de-peaking as well.

By using the published s-parameters for Q_1, Q_2, and Q_3, assuming all capacitances to be ideal, and all resistances to have their nominal value in parallel with a stray capacitance of 0.0826 pF which approximates the capacitance of the 0805-sized alumina chip that the thick-film resistors are fabricated on, it was possible to adjust all seven resistances and three gate peaking inductors to produce a calculated flat gain, or magnitude of overall s_{21}, of 20 dB and bandwidth of 6 GHz. Also, it was possible to determine a set of resistance and gate inductance values that produced 17.5 dB of gain up to 7 GHz. In both of these optimization runs, relatively low magnitudes for s_{11} and s_{22} were also specified as goals. The MDS design file that performed this task is quite large and detailed,

and appears in Appendix C. The resulting optimum resistance and inductance sets appear in Table 3.1.

	20 dB of gain and 6 GHz of bandwidth		17.5 dB of gain and 7 GHz of bandwidth	
	optimum value	nearest nominal value	optimum value	nearest nominal value
R_{g1}	245.1 Ω	220 Ω	184.3 Ω	200 Ω
R_{g2}	680.0 Ω	680 Ω	680.0 Ω	680 Ω
R_{g3}	177.2 Ω	200 Ω	187.9 Ω	200 Ω
R_{d1}	69.9 Ω	100 Ω	66.5 Ω	51 Ω
R_{d2}	50.6 Ω	51 Ω	39.3 Ω	47 Ω
R_{d3}	680.0 Ω	680 Ω	680.0 Ω	680 Ω
R_{g1s}	61.3 Ω	51 Ω	147.7 Ω	150 Ω
L_{g1}	0.20 nH	0.20 nH	0.96 nH	0.96 nH
L_{g2}	1.57 nH	1.57 nH	1.97 nH	1.97 nH
L_{g3}	0.20 nH	0.20 nH	0.24 nH	0.24 nH

Table 3.1. Optimum resistance and inductance values for the electronic amplifier

The calculated gain, input and output SWRs, and noise figure of the electronic amplifier with 17.5 dB of gain and 7.0 GHz of bandwidth appear in Figures 3.7a to 3.7 c. Also shown in Figure 3.7d is a low-frequency simulation which illustrates the low-frequency roll-off.

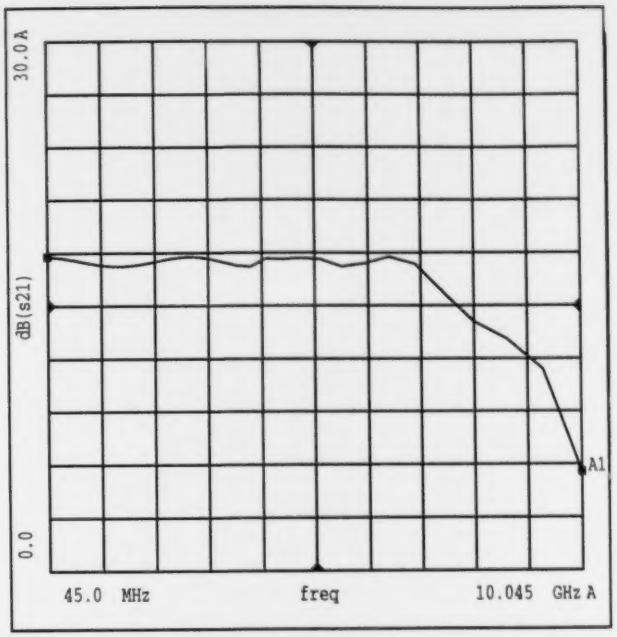


Figure 3.7a Calculated gain spectrum of electronic amplifier

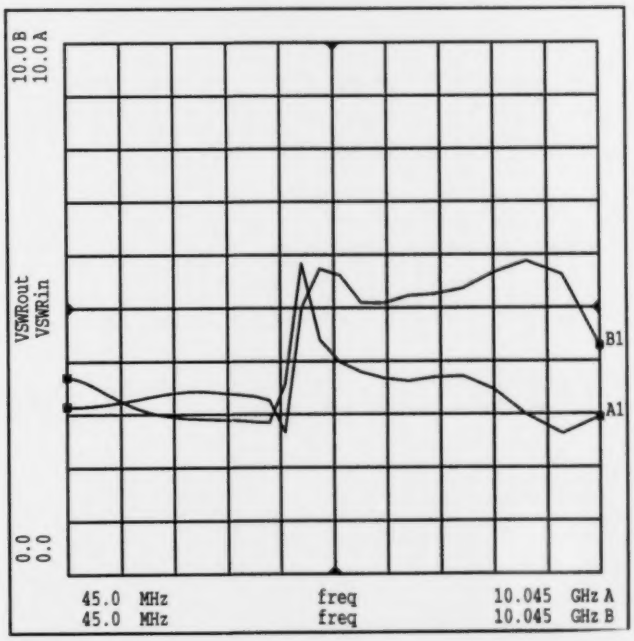


Figure 3.7b Calculated input (A1) and output (B1) SWRs of electronic amplifier

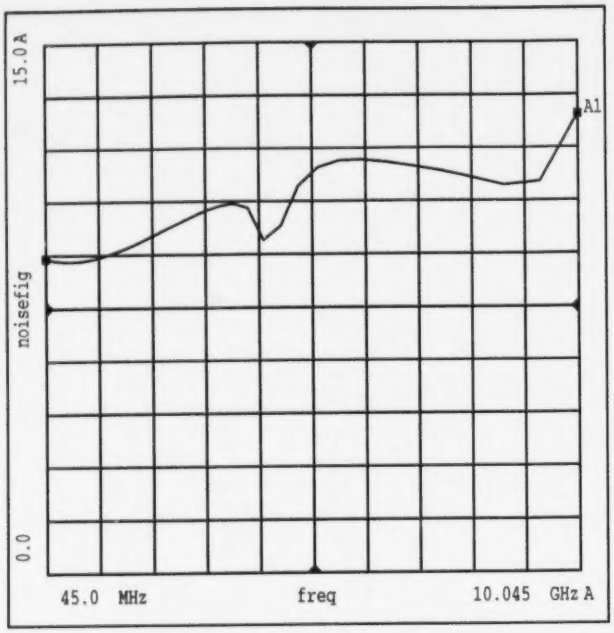


Figure 3.7c Calculated noise figure of electronic amplifier

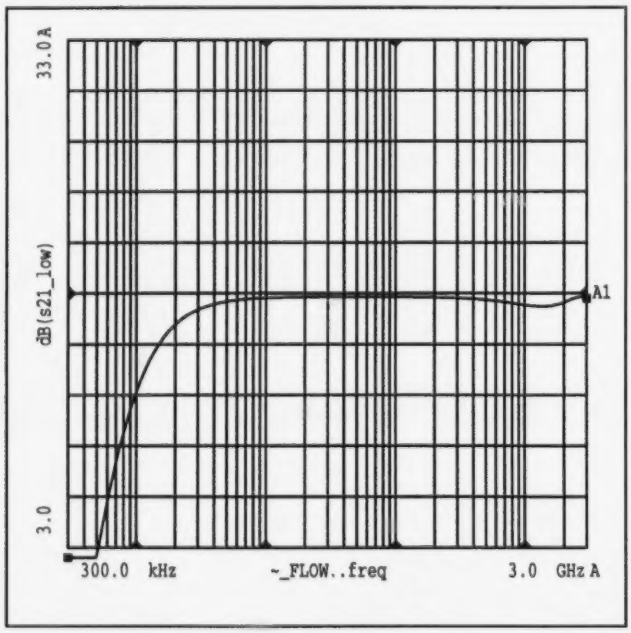


Figure 3.7d Calculated low frequency behavior of electronic amplifier

For the optimizations, all seven resistors were restricted to be in the range from 10 Ω to 680 Ω. Drain resistors cannot be more than 1000 Ω, because the 0805 chip resistors have a maximum rated power dissipation of 0.1 W, and the HEMTs require I_{DS} of 10 mA to operate. The upper limit of 680 Ω was chosen to provide a margin of safety, and also because the difference between 680 Ω and 1000 Ω for any resistor value in this amplifier configuration is negligible. Gate peaking inductances were limited to the range 0.20 nH to 2.5 nH, which was determined by the practical limits on bond wire lengths that can be installed at the gates of the HEMTs.

The same circuit configuration was optimized as a transimpedance amplifier. For this case, the s-parameter 50 Ω ports at the input and output were changed to a current source and a 50 Ω load resistor, and then an optimization was carried out with goals of 50 dBΩ for gain and 10 GHz for bandwidth. This succeeded, and the set of optimum resistance and peaking inductance values appears in Table 3.2 below. It was possible to achieve much more bandwidth with this configuration because an ideal current source matches much more easily to the gate-source port of a FET than does an electric source with a 50 Ω impedance.

	50 dBΩ of transimpedance and 10 GHz of bandwidth	
	optimum value	nearest nominal value
R_{g1}	69.9 Ω	100 Ω
R_{g2}	223.4 Ω	220 Ω
R_{g3}	346.1 Ω	330 Ω
R_{d1}	35.0 Ω	33 Ω
R_{d2}	81.7 Ω	51 Ω
R_{d3}	257.2 Ω	270 Ω
R_{g1s}	64.4 Ω	51 Ω
L_{g1}	0.58 nH	0.58 nH
L_{g2}	0.20 nH	0.20 nH
L_{g3}	0.29 nH	0.29 nH

Table 3.2 Optimum resistance and inductance values for the transimpedance amplifier

The calculated transimpedance in dBΩ and equivalent input noise spectral density in A/√Hz of the transimpedance amplifier with 50 dBΩ of gain and 10.0 GHz of bandwidth appear in Figures 3.8a and 3.8b.

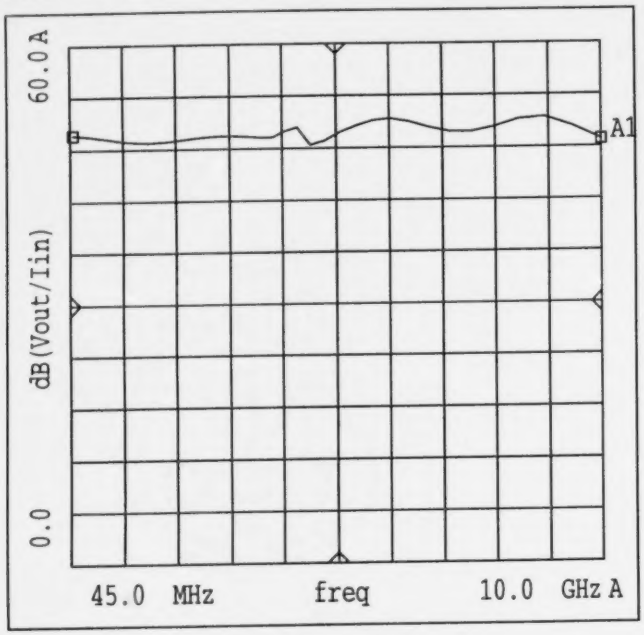


Figure 3.8a Calculated gain spectrum of transimpedance amplifier

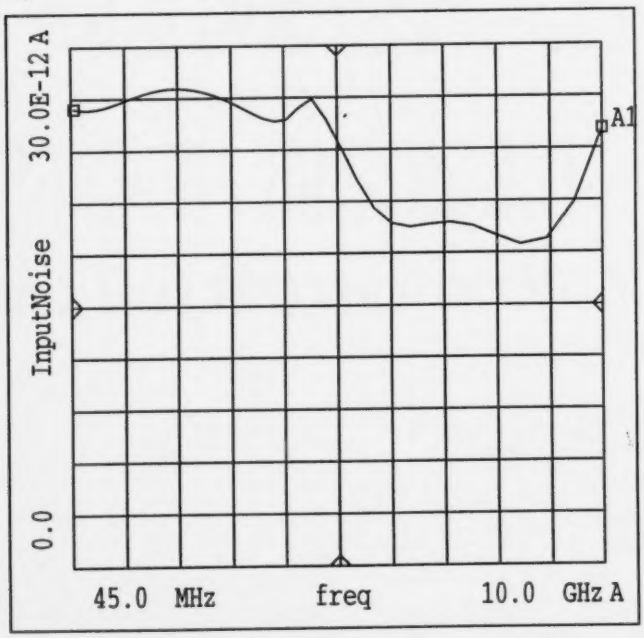


Figure 3.8b Calculated equivalent input noise spectral density

3.3 Circuit/Substrate Layout

MDS can create layouts automatically. There are built-in layout instances for all microstrip components, and layout instances for the 0805 chip components, bond wires, and HEMTs were developed. This resulted in a full-color view of the substrate and component layout before fabricating a mask. Software that automatically generates files that mask-making equipment can read, such as GDS or Gerber formats, from MDS layouts is also available, but was not used for availability and technical reasons. The layout of the circuit appears in Figure 3.9.

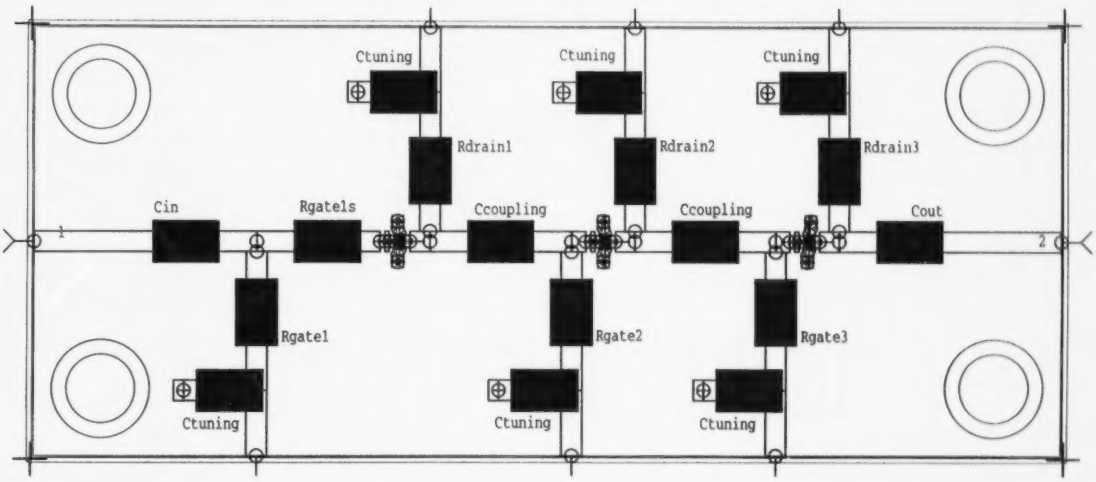


Figure 3.9. Complete electronic amplifier layout

3.4 Fabrication and Assembly

3.4.1 The Alumina Substrate

Originally, the MDS layout was translated manually to the L-Edit software package at the Alberta Microelectronic Centre (AMC), from which a GDS file was generated, sent to PPM Photomask in St.-Laurent, Quebec, who made a chrome-on-glass mask and then returned it to AMC where a chrome-gold photolithography run placed the pattern on 25-mil-thick, 2" by 2" alumina substrates. Then, the substrates were sent to Laser Process Technology (LPT) in Portland, Oregon, where the via holes were drilled using a carbon

dioxide laser. Upon return, AMC sawed the substrates, and then an attempt to fill the via holes with EpoTek's H20E two-part, heat cured conductive silver epoxy was made. This final step failed.

Then, Peter Borkowski at the Communications Research Centre (CRC) offered to fabricate substrates free of charge if provided with the mask. This resulted in the production of two satisfactory substrates, with very durable gold on chrome traces, ground plane, and plated-through via holes. Multiple wire bonding, silver epoxy cures and removals, and scraping with a steel blade left good traces to work with. Silver epoxy around the lips of the via holes was used to ensure good connection between the plating in the holes and the pads on the surface. In order to achieve good-quality, plated-through vias, holes were drilled larger than specified. All vias were 450 μm in diameter. Locations were determined such that these new, larger holes didn't obliterate the original source-grounding pads, yet still had some contact with the pads, without affecting near-by microstrip lines.

3.4.2 Assembling Components on the Substrate

It was decided to assemble the amplifier with the component values returned by the 17.5 dB/7.0 GHz electronic amplifier optimization, as meeting the bandwidth requirement was deemed more important than the gain requirement. The 7 GHz design allowed for a 1-GHz margin for the circuit to meet the bandwidth requirement.

The first components assembled to the substrate were the chip HEMTs. Then, using the K&S manual wedge bonder at AMC, 1.25-mil diameter 99.99% gold wire was used to connect the contacts on the HEMTs to the traces on the alumina substrate, rather than the 1.00-mil diameter wire as specified on the HEMT data sheet. One-mil wire was not available, and 0.7 mil wire was virtually impossible to work with. Also, this large-diameter wire would very slightly reduce unwanted bond wire inductance. For the gate peaking inductances, the loop of the bonds was set to result in bond wire pairs of approximately the correct length to provide the required inductance values.

All the 0805-size chip resistors and capacitors were cemented in place with the H20E silver epoxy.

3.4.3 The Aluminum Packaging

The packaging of the electronic amplifier is shown in Figure 3.10.

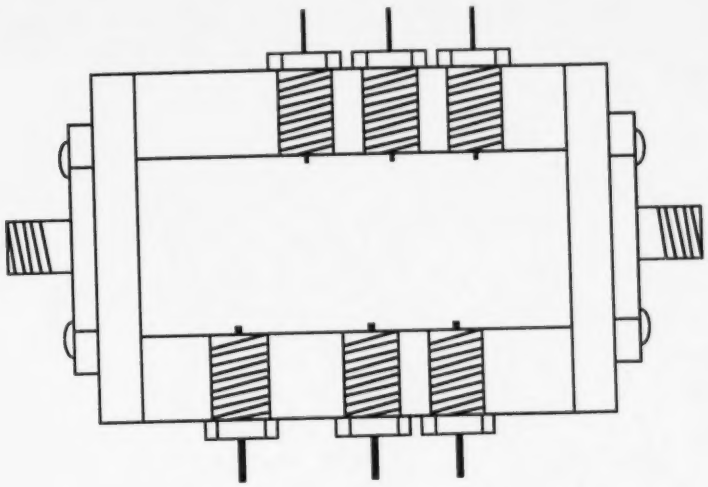


Figure 3.10 The electronic amplifier package

This aluminum package was in three pieces. The alumina substrate fits on the floor of the large middle piece, into which feedthrough capacitors were screwed. The inside leads were cut short and connected to the bias line traces on the substrate with conductive epoxy. Gold-plated female SMA sockets fit into each of the two end pieces, with the centre conductors connected to the input and output traces on the substrate with conductive epoxy. The two end pieces are held to the large middle piece with two screws apiece.

When configured as an optical receiver, the input end piece of the electronic amplifier package is removed and another aluminum package that holds an alumina substrate containing a 1 by 8 MSM array is butted up against the main package piece. On the alumina substrate which holds the MSM array there are bias lines which connect at one end to the individual MSM pads through gold bond wires. A 50 Ω microstrip trace is connected to the common MSM strip through several gold bond wires, and then to the amplifier input through conductive epoxy. Also connected to the common MSM strip is a pair of gold wires leading to a 200 Ω resistor which is then grounded through a via hole. This provides a DC path to ground for the MSM bias voltages. This arrangement is shown in Figure 3.11.

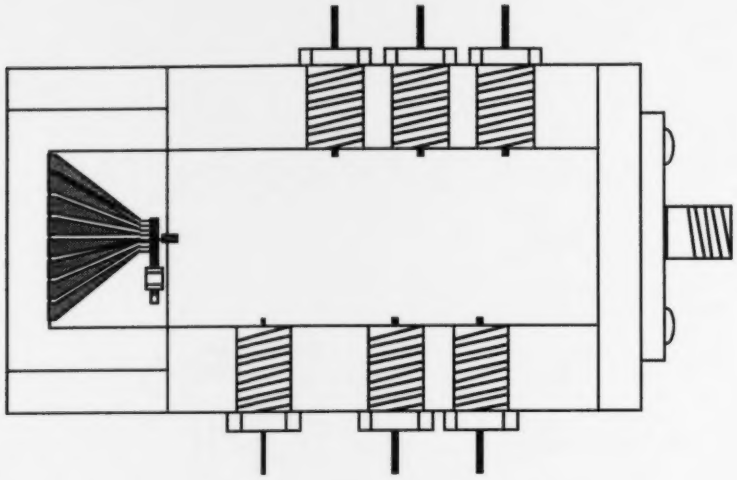


Figure 3.11 The optical receiver in its package

3.5 DC Biasing

The necessary DC bias voltages were calculated by substituting the required drain-source current (I_{DS}) of 10 mA, the rated maximum drain-source current (I_{DSS}) of 30 mA, and the typical pinch-off voltage (V_p) of -0.7 V to -0.55 V into [23]

$$V_{GG} = V_p\left(1 - \sqrt{\frac{I_{DS}}{I_{DSS}}}\right)$$

to achieve a required range of -0.30 V to -0.23 V for the three gate bias voltages V_{GG1}, V_{GG2}, and V_{GG3}. Drain bias voltages are simply $V_{DDn} = 2.0\text{ V} + R_{dn}(10\text{ mA})$ for the three stages n = 1, 2 and 3. It is important when applying bias that the gate voltages be turned on before the drain voltages, otherwise the HEMTs will be destroyed by excessive channel current.

4. Measured Results

4.1 Measured Gain of Electronic Amplifier

After applying the six DC bias voltages to the electronic amplifier and connecting it to a calibrated HP 8510B network analyzer, the initial measured results were poor. Gain, which is $20\log_{10}|s_{21}|$, expressed as dB, was not flat at all, as Figure 4.1 shows.

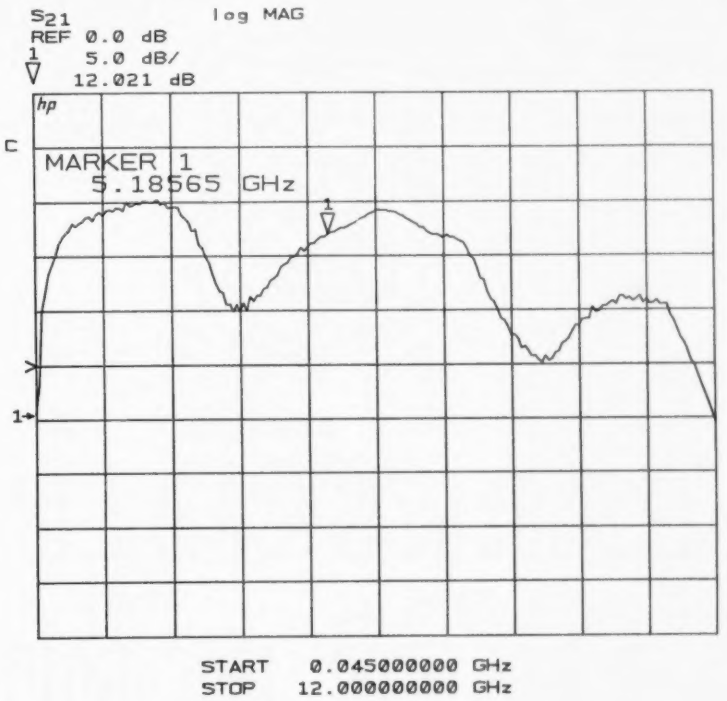


Figure 4.1 Initial measurement of s_{21}, in dB

This was discouraging, but there was reason for optimism. Even though the gain was variable over the expected passband, there was positive gain up to 8 GHz. As was stated earlier, changing bias resistor values and tuning capacitor values were expected to correct any problems due to unaccounted-for parasitics in the design, active device variability, and any other unforeseen circumstances.

Cursory investigations revealed that poor substrate grounding and some poor conductive epoxy connections were partly responsible for the initial result. In an attempt to remedy these problems, holes drilled in the floor of the main package piece, from an early via hole grounding scheme that didn't work, were partly filled with conductive epoxy to

lessen spurious responses caused by these cavities. The floor of the main package piece was carefully sanded to make it smoother to provide a better contact to the substrate ground plane. Poor conductive epoxy connections, notably on the output SMA centre conductor, were corrected.

Most importantly, tuning devices were constructed. In order to gauge the effect of changing bias resistor and tuning capacitor values, existing resistor and capacitor values had to be changed. In order that this be accomplished quickly, removing and re-cementing resistor and capacitor chips was not an option. Instead, "tuning sticks" were created. These consisted simply of wooden toothpicks with various 0805-size chip capacitors and resistors held on one end by silicone. By using these devices, existing resistor and capacitor values could be quickly changed by carefully placing other resistors and capacitors values over top with these sticks. The wood and silicone has no effect on circuit performance, and conductive epoxy bumps added to the metal contacts on the chips are necessary due to the raised, protective glaze on the tops of the chip resistors. This worked very well. After a time, a flatter gain spectrum was achieved, as illustrated in Figures 4.2 and 4.3.

The general procedure followed in tuning the amplifier first involved changing the bias resistor values. Since resistances could only be added in parallel to existing resistances, this step resulted in a lowering and flattening of gain, and this was effective in the frequency range up to about 2.5 GHz. Beyond this frequency, adding capacitances on the order of picofarads across bias resistors flattened gain from 2.5 GHz to about 4.5 GHz. Above 4.5 GHz, unwanted peaking was flattened by adjusting tuning capacitance values. The net result is a general, empirical procedure that worked well to flatten the gain spectrum of the amplifier over its entire bandwidth.

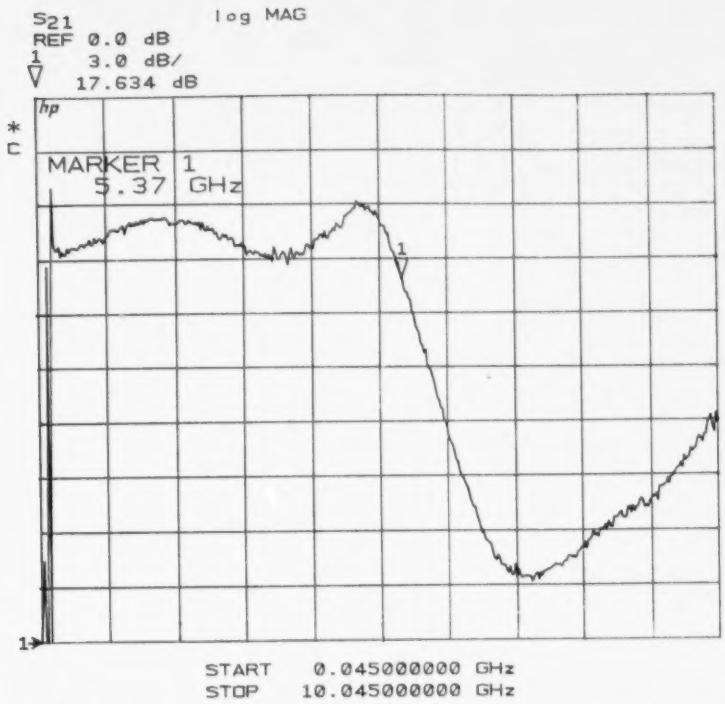


Figure 4.2 Gain spectrum, exhibiting 3-dB ripple up to 5 GHz

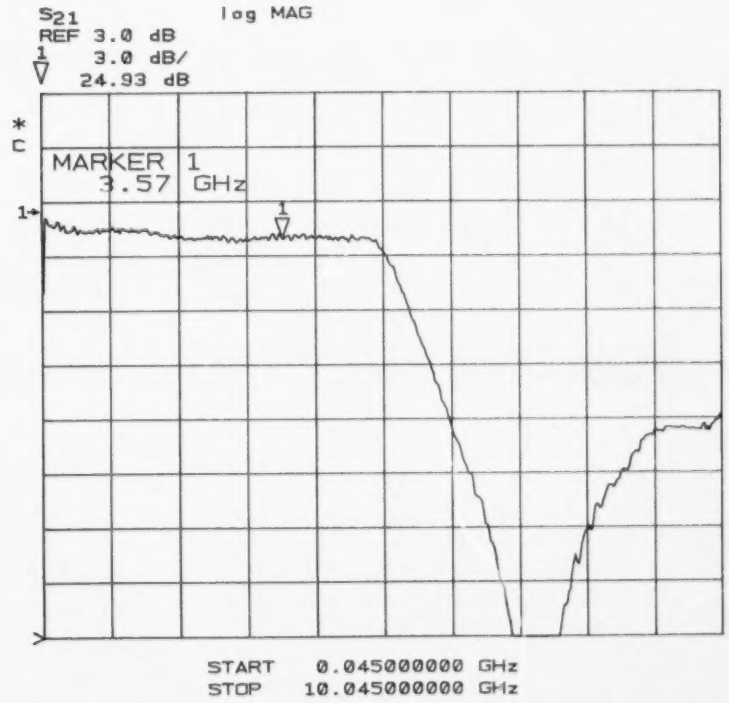


Figure 4.3 Gain spectrum, exhibiting 0.75 dB of ripple up to 5.37 GHz

Finally, the gain that was realized was 25.0 dB, with 0.75 dB of ripple from very low frequencies up to the 3 dB-down bandwidth of 5.37 GHz. This result was not the original goal, which was 17.5 dB gain up to 7 GHz, but by this time several passive circuit components had been changed or removed. The revised circuit is shown in Figure 4.4.

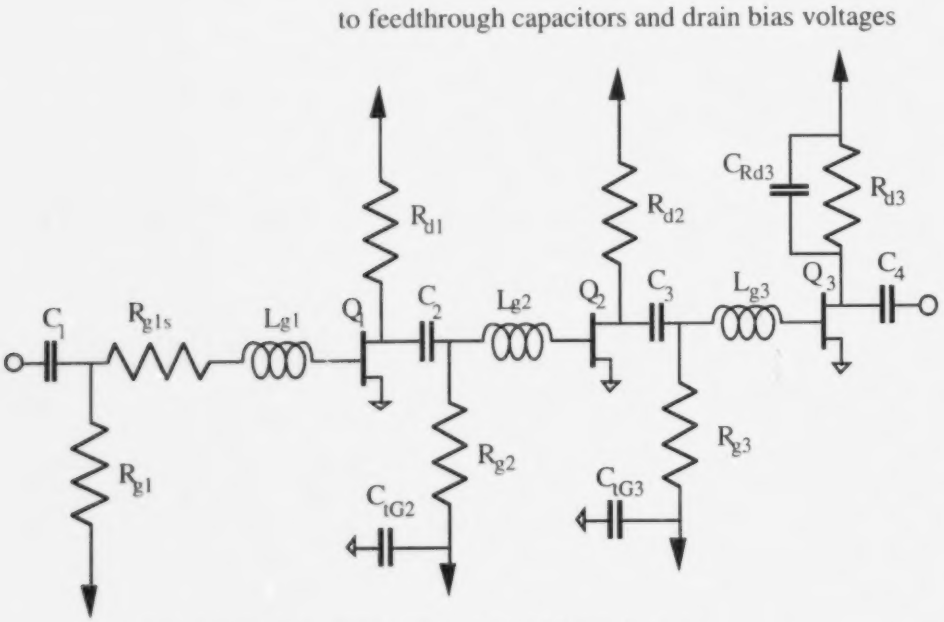


Figure 4.4 Simplified circuit diagram of electronic amplifier that produces the response of Figure 4.3

The transistors Q_1 and Q_2 are FHX 06X HEMTs, and Q_3 is an FHX 04X. The resistor values are R_{g1s} = 10 Ω, R_{g1} = 200 Ω, R_{g2} = 680 Ω, R_{g3} = 200 Ω, R_{d1} = 51 Ω, R_{d2} = 47 Ω, and R_{d3} = 51 Ω. The gate peaking inductors were fabricated to be approximately equal to the design values. The capacitor values are C_{Rd3} = 1.0 pF, C_{tG2} = 4.7 pF, C_{tG3} = 1.0 pF, and C_{tD1}, C_{tD2}, C_{tD3}, and C_{tG1} are all removed. Bias voltages had changed, too: V_{GG1} = -0.14 V, V_{GG2} = -0.14 V, V_{GG3} = -0.24 V, V_{DD1} = 2.45 V, V_{DD2} = 2.45 V, and V_{DD3} = 2.08 V. This made the drain-source voltages V_{DS1} = 1.32 V, V_{DS2} = 1.39 V, and V_{DS3} = 0.98 V. These are the bias voltages that force this circuit to have a maximum flat gain of 25.0 dB in the passband. Adjusting the bias voltages to achieve the bias points prescribed in the transistor data sheet, namely I_{DS} = 10 mA and V_{DS} = 2 V, results in a gain of about 21.0 dB in the passband, while still maintaining the same bandwidth of Figure 4.3. This lower response is shown in Figure 4.5.

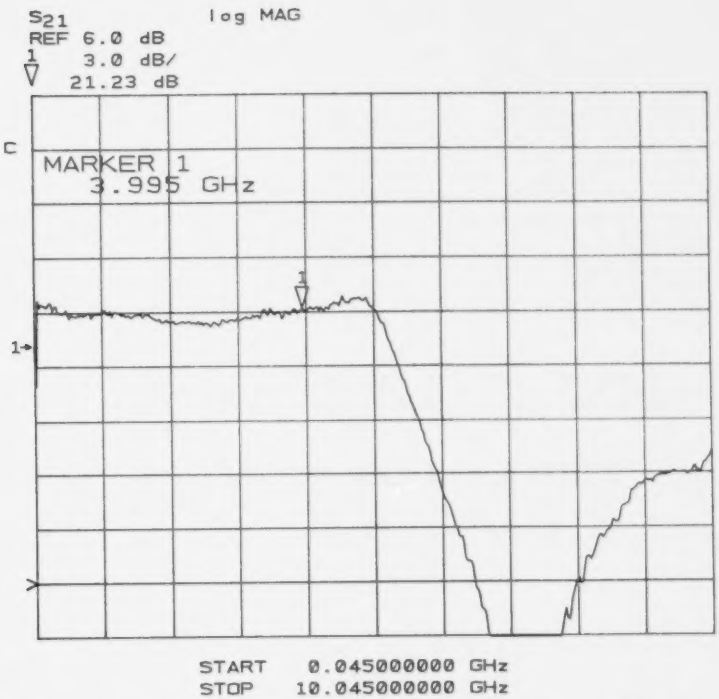


Figure 4.5 Gain spectrum for I_{DS} = 10 mA and V_{DS} = 2 V for each stage

Essentially, the gate bias voltages can be altered by a few tenths of a volt from the above nominal values, and drain bias voltages can be increased by a volt or two, without changing the gain spectrum. But such changes alter the amplitude by several dB, from values in the high teens to the maximum value of 25.0 dB.

4.2 Input and Output Reflections (SWRs)

The measured input and output SWRs are shown in Figures 4.6 and 4.7. The input SWR became unexpectedly small above 4 GHz, and the output SWR is much smaller than expected over the entire frequency range of the measurement, due to the change of R_{d3} from the design value of 680 Ω to the actual value of 51 Ω.

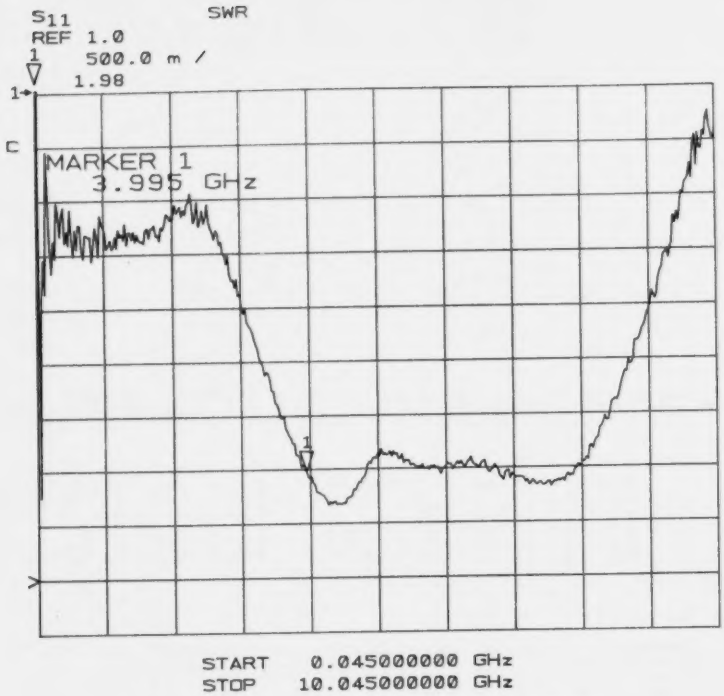


Figure 4.6 Measured input SWR

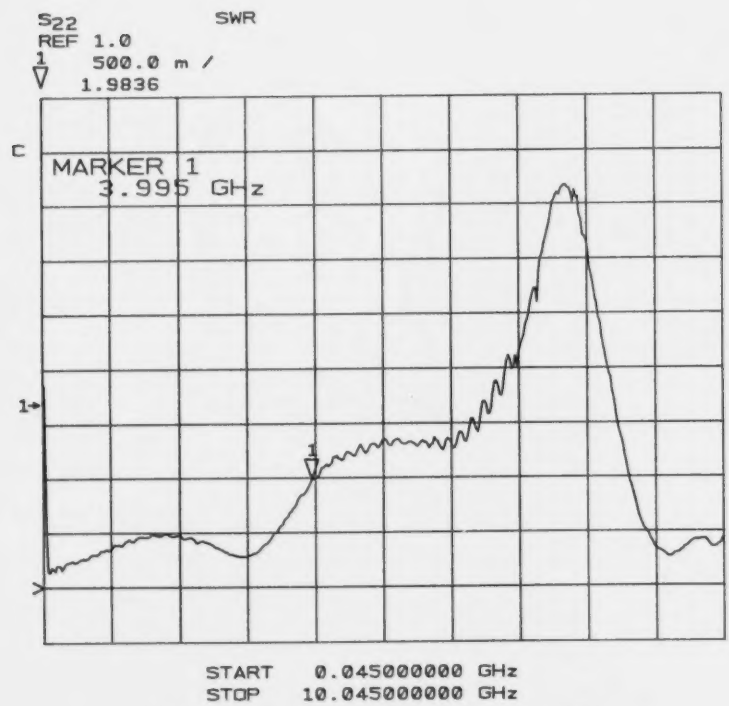


Figure 4.7 Measured output SWR

At frequencies less than about 2 GHz, the value of the input SWR = 4 ≈ (200 Ω + 50 Ω)/(200 Ω - 50 Ω) = 5, where 50 Ω is the input impedance to the s-parameter test set port one and 200 Ω is the value of R_{g1}. Similarly, output SWR of just over one at frequencies of less that about 2 GHz is due to R_{d3} = 51.0 Ω.

4.3 Measured Low Frequency Response

As Perennec states in [12] and [13], in very high data rate optical systems, amplifiers must have a bandwidth of at least three decades. Using 1.0 nF coupling capacitors, calculations and simulations showed that there would be no problem in meeting this requirement. The measurements revealed one problem, illustrated in Figure 4.8.

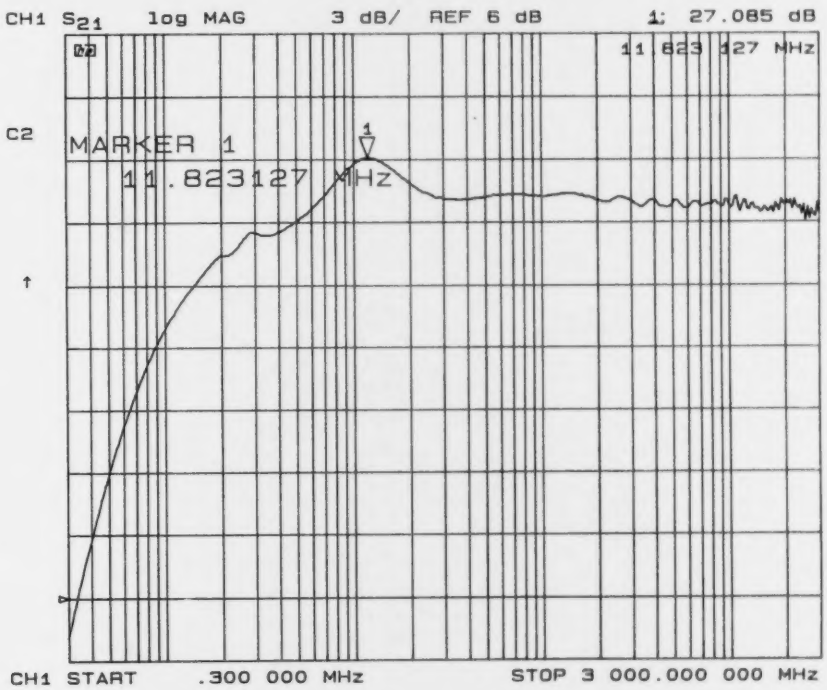


Figure 4.8 Measured low frequency gain, from 300 kHz to 3 GHz

In the original measurement, a large peak of magnitude greater than 40 dB appeared at 11.8 MHz . This peak was probably due to the formation of a resonance down the bias paths inside the package at this frequency. In order to decrease this peak to the magnitude shown in Figure 4.8, which is about 2 dB above passband gain, large capacitances were added between the centre conductors of the feed-through capacitors on the exterior of the

package and the package itself, which would then provide a very short path to ground for the frequencies of the peak. Electrolytic capacitors C_{D1} = 10 μF, C_{D2} = 33 μF, C_{D3} = 22 μF, and C_{G1} = 10 μF were used, where the subscripts D and G indicate whether the capacitors were added to the gate or drain side, and 1, 2, and 3 refer to the stage number. Capacitances at these points were highly effective due to the low values of the drain bias resistors and the relatively low R_{g1} of 200 Ω. The measured low end 3 dB-down frequency of about 2 MHz easily meets the three-decade bandwidth requirement.

4.4 Phase Linearity and Group Delay

It is important that the phase response of the amplifier be very linear, otherwise the frequency components of multi-Gbit/s digital signals will travel at different speeds through the device, resulting in significant intersymbol interference (ISI). Another way of expressing this idea is with the concept of group delay, defined as $-\partial(\text{phase}[s_{21}])/\partial f$, which is constant if phase response is linear. Measurements of phase of s_{21} and group delay are presented in Figures 4.9 and 4.10, and show linear phase response in the passband.

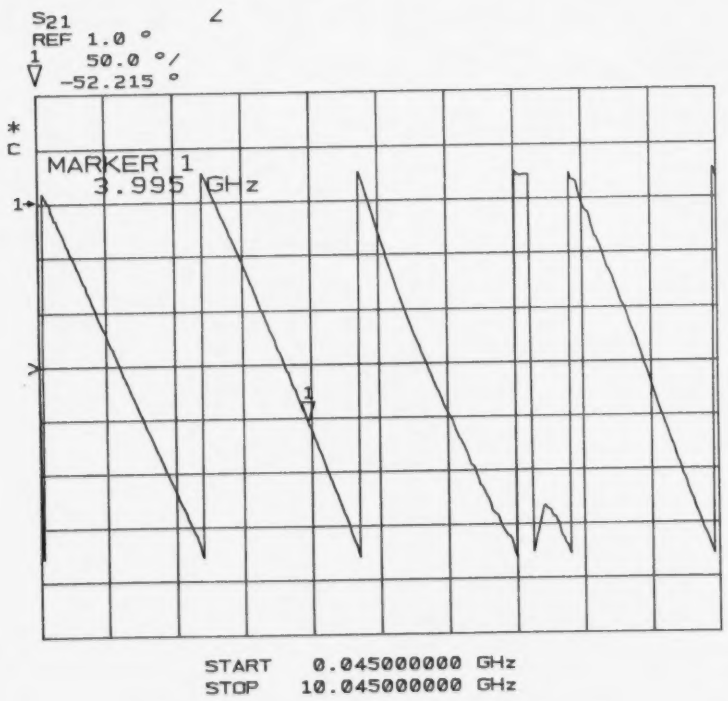


Figure 4.9 Measured phase of s_{21}

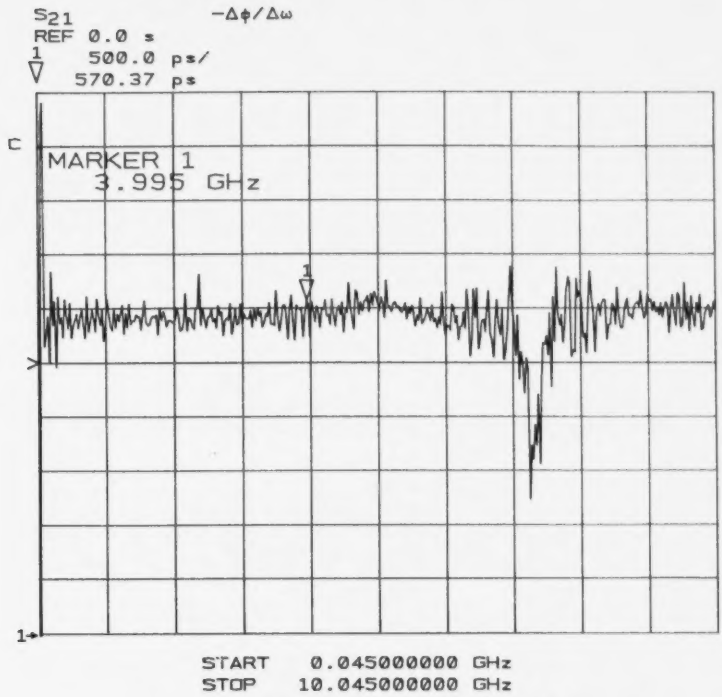


Figure 4.10 Measured group delay

4.5 Noise Figure Measurements

In order to perform a noise figure measurement of the amplifier, it was necessary to use a spectrum analyzer with a known noise characteristic, then apply a well-known relation for determining the noise figure for a cascade of noisy two-port devices [24] as shown in Figure 4.11.

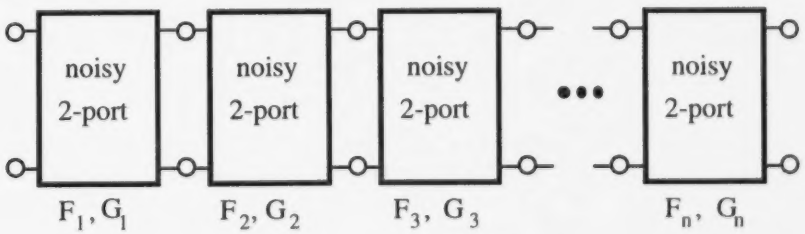


Figure 4.11 Cascade of noisy 2-port networks

For the cascade of noisy two-port networks of Figure 4.11, each with gain G_i and noise figure F_i, $\{i = 1,2,...n\}$, the noise figure of the cascade is given by

$$F_{cascade} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}}.$$

In this case, the cascade is of two devices: first, the amplifier, making F_1 and G_1 above become F_{amp} and G_{amp}, and the HP 71000 series spectrum analyzer, turning F_2 and G_2 into F_{sa} and G_{sa}. Therefore

$$F_{amp} = F_{cascade} - \frac{F_{sa} - 1}{G_{amp}},$$

where F_{amp} is the noise figure of the amplifier, $F_{cascade}$ is the noise figure of the amplifier and spectrum analyzer cascade, F_{sa} is the noise figure of the spectrum analyzer alone, and G_{amp} is the gain of the amplifier.

First, the noise figure of the spectrum analyzer must be determined. This is accomplished with the experimental set-up shown in Figure 4.12.

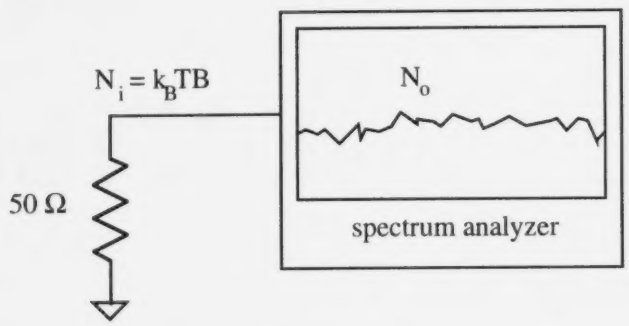


Figure 4.12 Set-up for determining noise figure of the spectrum analyzer

N_o is the measured noise spectrum of the spectrum analyzer with a 50 Ω load connected to its input. Due to the unity gain of the spectrum analyzer, its noise figure is

$$F_{sa} = \frac{N_0(\text{measured})}{N_i},$$

where $N_i = k_B TB$, Boltzmann's constant $k_B = 1.38 \times 10^{-23}$ J/°K, room temperature T = 300°K and bandwidth B = 1.0 Hz. The input noise N_i is -173.8 dBm, or 173.8 dBm/Hz because noise is calculated in a 1 Hz bandwidth.

For the frequency range of 45 MHz to 10.045 GHz, it is possible to determine the noise figure of the spectrum analyzer by simply observing N_o on the spectrum analyzer display, and substituting it into the expression for F_{sa} above. This result is shown in Figure 4.13.

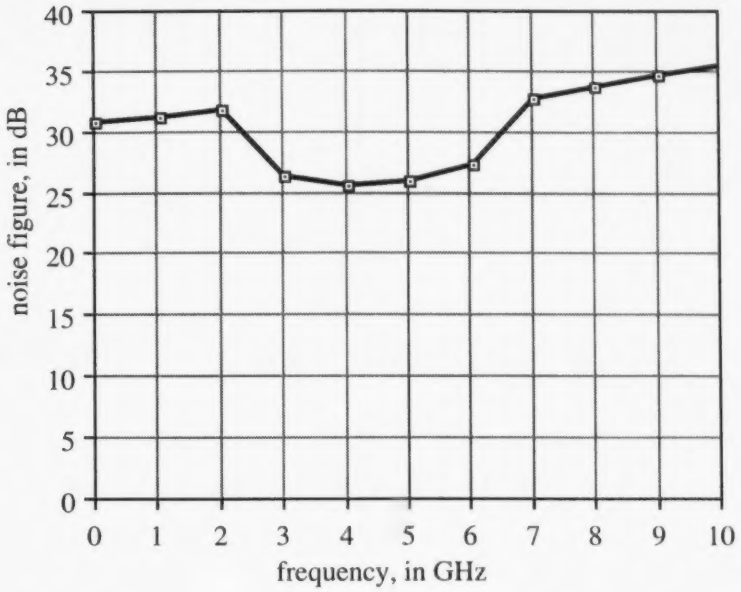


Figure 4.13 Measured noise figure of HP 71000 spectrum analyzer

The noise figure of the amplifier is determined by observing the noise spectrum of the cascaded amplifier and spectrum analyzer with a 50 Ω termination at the input, and all bias voltages applied. Noise generated by a MESFET is a function of bias condition [25]. The experimental set-up for this measurement is depicted in Figure 4.14.

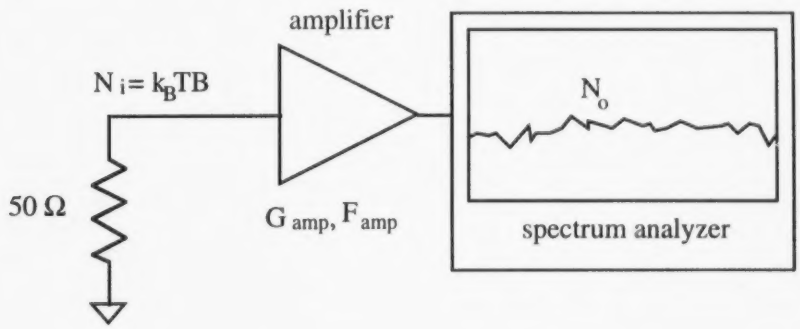


Figure 4.14 Set-up for determining noise figure of the amplifier

Again, $F_{cascade} = N_o/N_i$. Substituting this measurement into the expression for F_{amp} above, the noise figure of the amplifier is determined, and is shown in Figure 4.15.

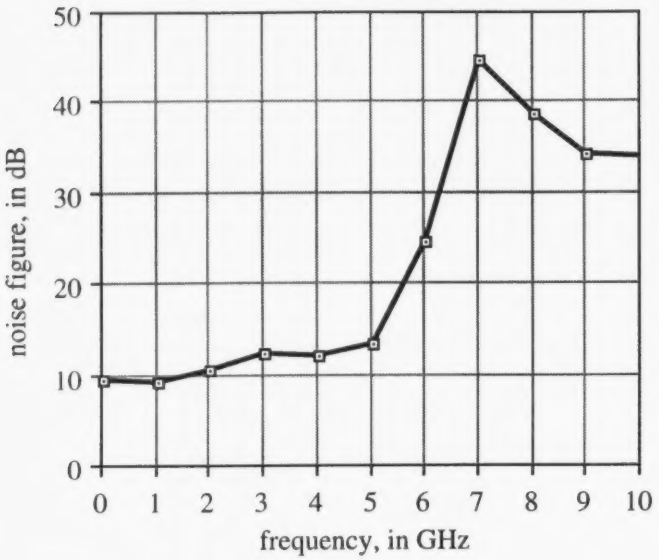


Figure 4.15 Measured noise figure of amplifier

In the passband, the measured noise figure is about 9 to about 12 dB, which is approximately equal to the calculated noise figure given in Figure 3.7c.

4.6 Output Power and Gain Compression

Using the HP 8510B network analyzer as a continuous wave (CW) microwave power source and the HP 71000 spectrum analyzer to measure power, it was possible to examine the gain linearity of the amplifier and determine its 1-dB and 3-dB gain compression points. Output power vs. input power and gain vs. input power measurements were taken at two frequencies, 2.0 GHz and 4.0 GHz, and the results are shown in Figures 4.16 and 4.17.

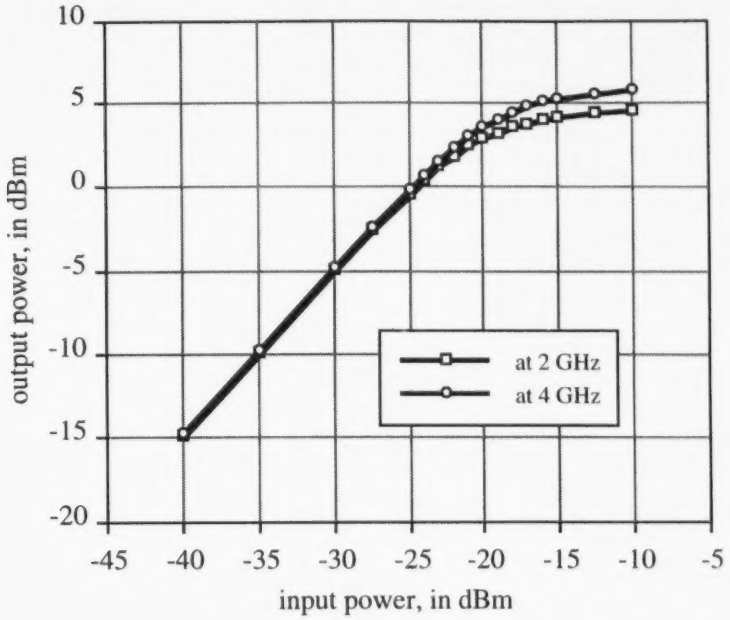


Figure 4.16 Measured output power vs. input power at 2 and 4 GHz

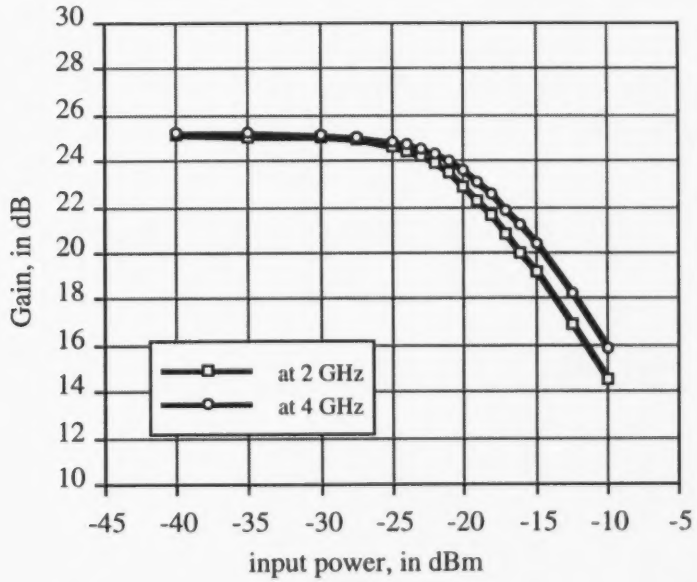


Figure 4.17 Measured gain vs. input power at 2 and 4 GHz

At 2 GHz and at 4 GHz, the output powers for which gain falls by 1 dB and 3 dB, or the 1-dB and 3-dB gain compression points, are summarized in Table 4.1 below.

	P_{out} at 1-dB gain compression point	P_{out} at 3-dB gain compression point
2.0 GHz	1.2 dBm	3.3 dBm
4.0 GHz	2.35 dBm	4.54 dBm

Table 4.1 Summary of gain compression points

Between the time that the output power and gain compression measurements were taken and the decision made to carry out more of these measurements at other frequencies, the first stage transistor failed. The gate-source junction shorted, so it was not possible to investigate this phenomenon further with this amplifier. Also, it was expected that the power output of the amplifier at the 1-dB and 3-dB gain compression points would be a few dBm more than what was observed, because the output power curve on the FHX 04X data sheets shows linear gain for output power up to approximately 10 dBm at 12 GHz. Comparisons between these measurements and predicted values were not made because output power calculations could not be carried out. Small-signal s-parameters of the transistors were the only information available for amplifier design.

4.7 The Second Electronic Amplifier

4.7.1 Reproducible Gain Spectrum

Upon the failure of the original amplifier, a repair was undertaken. The first stage transistor was removed and replaced with an FHX 04X HEMT. This required a disassembly of the substrate from the package, removal of the failed transistor, and installation of the new one, including wire bonding and a re-fabrication of L_{g1}. After complete re-assembly and some empirical re-tuning, the response of the original amplifier was very nearly re-created, as shown in Figure 4.18.

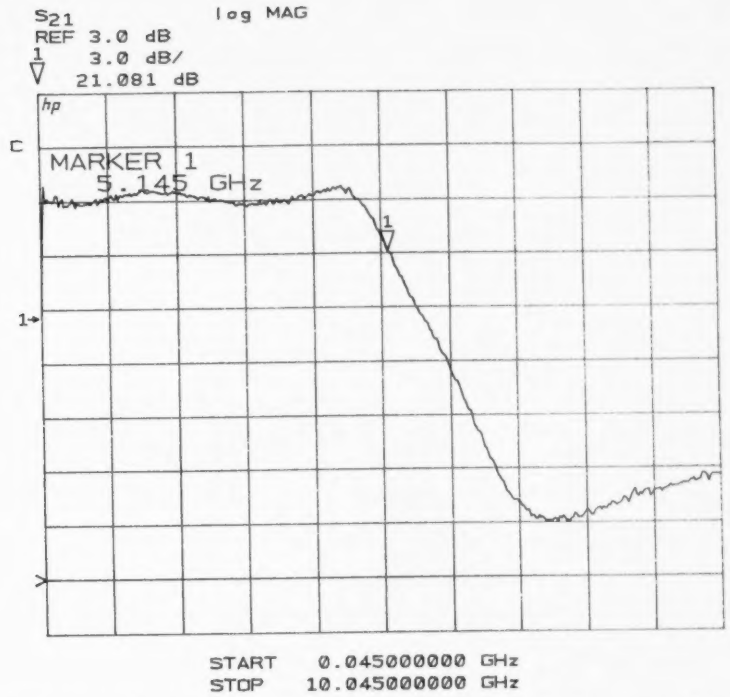


Figure 4.18 Measured frequency response of the second amplifier

Passband gain of 24.5 dB was measured, with gain ripple of 1 dB. The high-frequency 3 dB-down point is at 5.1 GHz.

One of the important results that emerged from this repair is that it is definitely possible to fabricate more of these amplifiers. Commercial-level quantities in the hundreds would be unrealistic, but a half dozen or so of these amplifiers could be made by a researcher for experimental purposes. Experience gained from empirically tuning the first amplifier led to this second one being realized in a few days, rather than the few weeks required for tuning the first one.

4.7.2 Noise Figure Dependence on First Stage Components

Using an FHX 04X HEMT for the first stage instead of an FHX 06X resulted in the measured noise figure of this second amplifier being a little higher than that of the first amplifier, even though a larger R_{g1} of 470 Ω was used. The measured noise figure of the second electronic amplifier is shown in Figure 4.19.

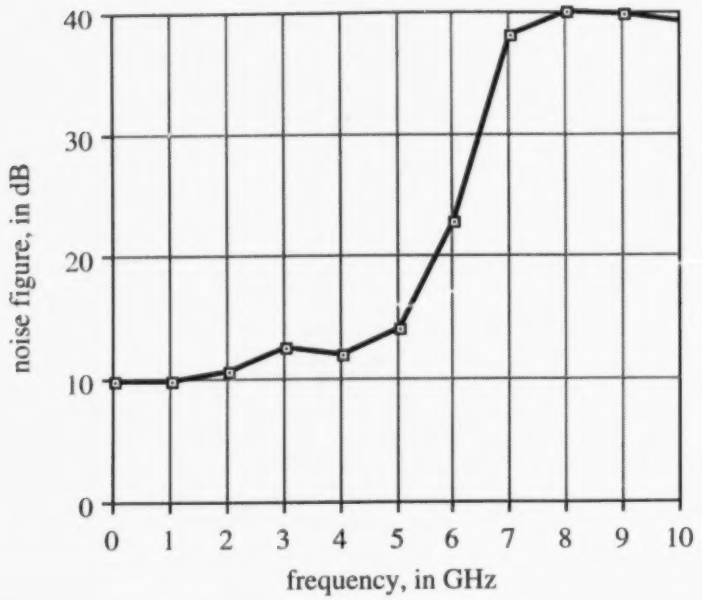


Figure 4.19 Measured noise figure of second amplifier

The reason for this is the difference between the minimum noise figure specifications of the FHX 04X and FHX 06X HEMTs on the data sheets sent with the devices, which is contrary to the information contained on the data sheets from Fujitsu's catalog. The actual measured minimum noise figures of the FHX 06X HEMTs are lower than those of the FHX 04Xs, while the reverse is true on the catalog data sheets. The reason for this may be inferred from the specification sheet test dates: 1991 for the FHX 04X HEMTs and 1993 for the FHX 06X HEMTs. Perhaps the processing steps involved in fabricating these devices are being refined over time, resulting in transistors with lower and lower noise as time passes.

4.8 Simulated Eye Diagram

The original design goal for bandwidth was 6.0 GHz. This goal was not quite met, with measured bandwidths of 5.37 GHz and 5.1 GHz for the two electronic amplifiers. However, this bandwidth goal was set to achieve amplification of a 10 Gbit/s NRZ binary signal, for which a theoretical minimum of 5.0 GHz bandwidth is required, so the possibility exists that the amplifiers could reliably pass a 10 Gbit/s NRZ signal. It was

possible [26] to simulate the eye diagram that would be produced by the measured response of the second amplifier.

The steps involved to produce the calculated eye diagram is as follows. First, a random 10 Gbit/s time domain signal was formed, then converted to its frequency domain representation by applying a discrete Fourier transform (DFT). Next, the frequency domain response of the amplifier is interpolated to have the same number of points in the frequency domain as the DFT of the input signal. Multiplying these two frequency domain responses together produces the frequency spectrum at the output of the amplifier, from which the time domain output is calculated by applying an inverse DFT. The eye diagram is formed by overlapping many short durations of the output time domain signal equal to an integral number of bit times on top of each other. These calculations were carried out using Matlab software, and the programs which generate the eye diagram in Figure 4.20 appear in Appendix D.

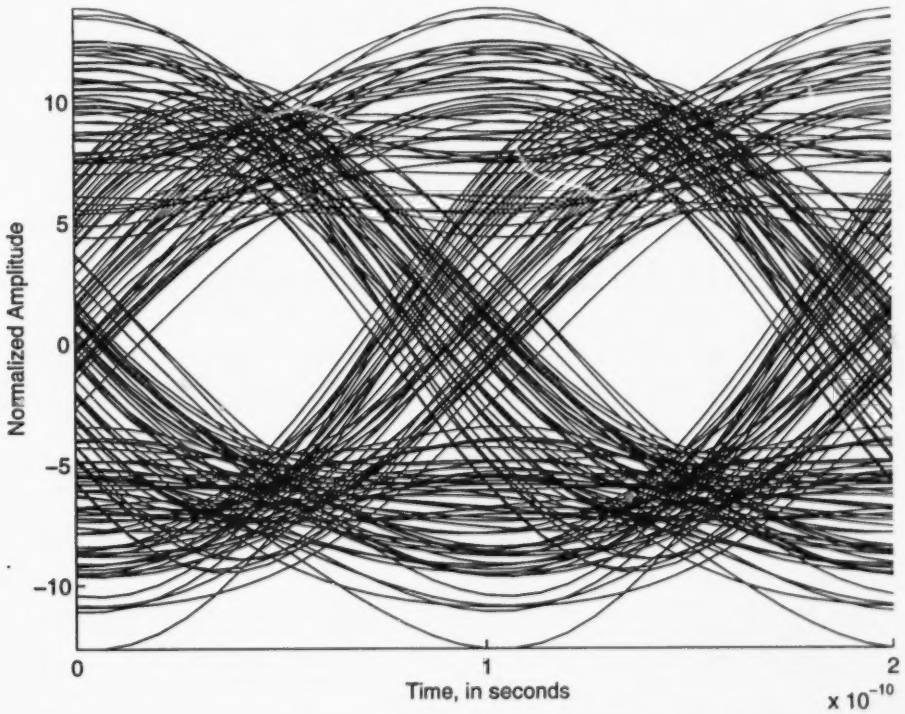


Figure 4.20 Simulated 10 Gbit/s eye diagram for second amplifier

For 10 Gbit/s, the eye is open. Further study revealed that lower bit rates around 5 Gbit/s had eyes which were nearly square, and at 11 Gbit/s, the resulting eye was almost completely closed.

4.9 Optical Receiver Measurements

The reconfiguration of the electronic amplifier as an optical receiver is achieved by removing the input end piece of the electronic amplifier package and replacing it with the 1 x 8 GaAs MSM array which was described in section 2.5. The common MSM connection is connected to a 50 Ω microstrip line on an alumina substrate through several gold bond wires, which is then butted against the 50 Ω microstrip line on the input side of the amplifier. Connection is made to the amplifier with conductive silver epoxy. Also, the common MSM connection is grounded through two gold bond wires, a 200 Ω 0805-sized chip resistor, and a 450 μm diameter via hole. This arrangement provides a DC path to ground when 5 V bias is applied to each individual MSM. The individual MSMs are connected through single gold bond wires to eight individual bias line traces on the alumina substrate. All this is illustrated in Figure 4.21.

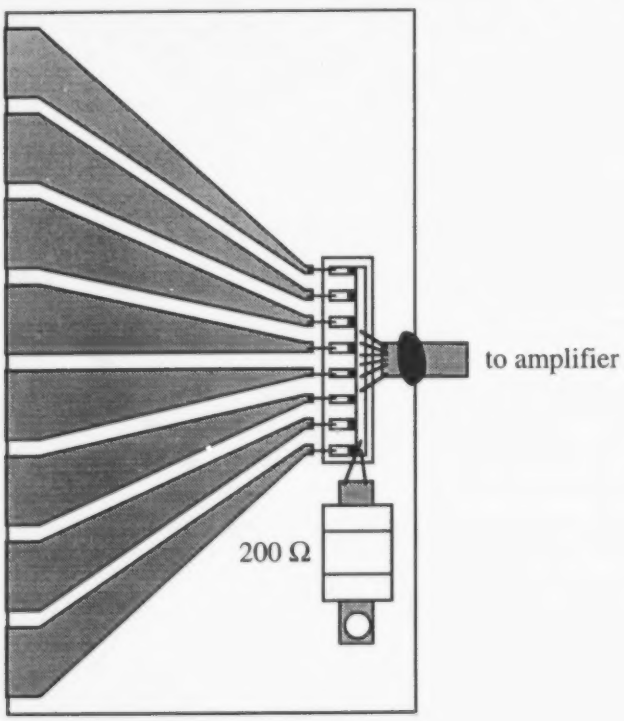


Figure 4.21 The 1 x 8 GaAs MSM array acting as input for optical receiver configuration

In order to measure the response of this arrangement, an amplifier substrate was built up with the nearest optimum resistor values, connected to the MSM array arrangement, and taken to the communication laboratory at the University of Saskatchewan in Saskatoon, where there is an externally modulated laser diode than can operate at frequencies up to at least 10 GHz. The experimental set-up is shown in Figure 4.22, with the optical connectors neglected.

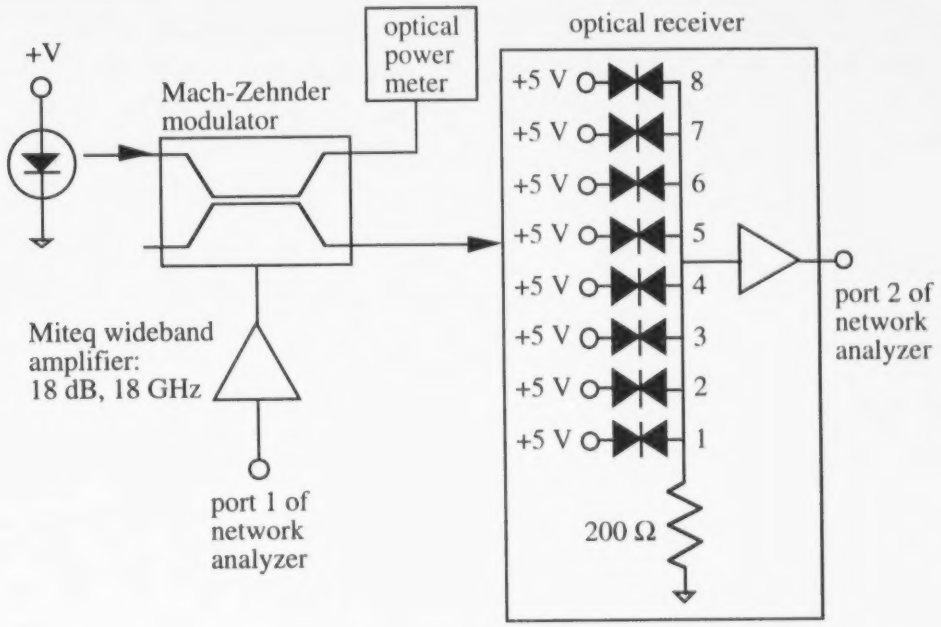


Figure 4.22 High-frequency optical experimental set-up in Saskatoon

A SeaStar laser diode biased at 53.2 mA at an operating temperature of 25 °C produces about 3 mW of light output at a wavelength of 835 nm. This is fed into a Mach-Zehnder optical modulator, which is driven by port 1 of an HP 8510B network analyzer through a wideband amplifier, which produces the necessary RF power to drive the modulator. One of the complementary outputs of the modulator is monitored by an optical power meter, and is maintained at approximately 0.5 mW, allowing 0.5 mW of light to exit the other modulator output and strike one of the MSM PDs at the input to the optical receiver. The second port of the network analyzer is connected to the output of the receiver.

The overall system was calibrated with a commercial wideband detector having a responsivity of 0.13 A/W. With only this detector and no amplification, the HP 8510

displays a flat s_{21} of 0 dB. After biasing and illuminating the third MSM in the array, and applying similar empirical tuning techniques to the optical receiver as applied to the electronic amplifier earlier, the frequency response shown in Figure 4.23 was attained.

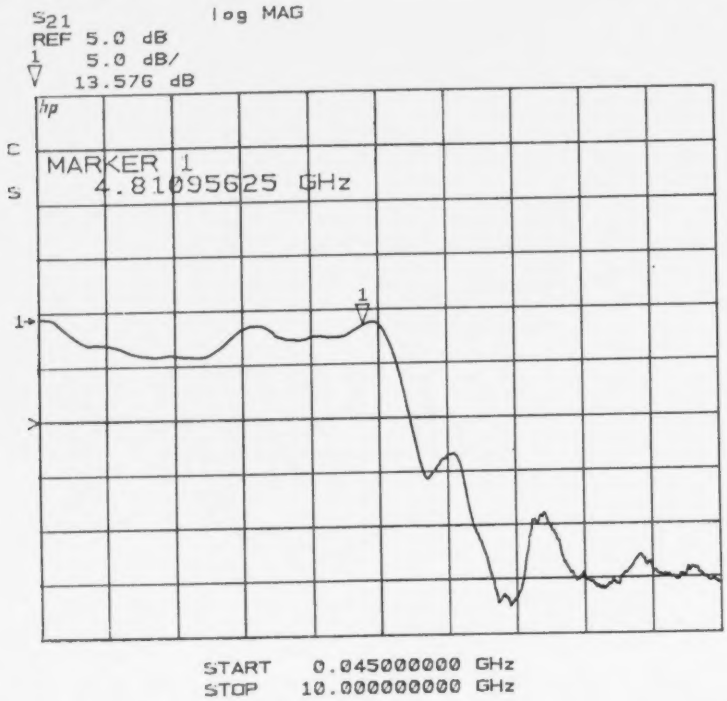


Figure 4.23 Gain spectrum of tuned optical receiver with third MSM illuminated.

The gain ripple is about 3.5 dB in the passband, and the 3 dB-down bandwidth is approximately 5.3 GHz.

The schematic diagram of the amplifier portion of the optical receiver that produced the response of Figure 4.23 appears in Figure 4.24.

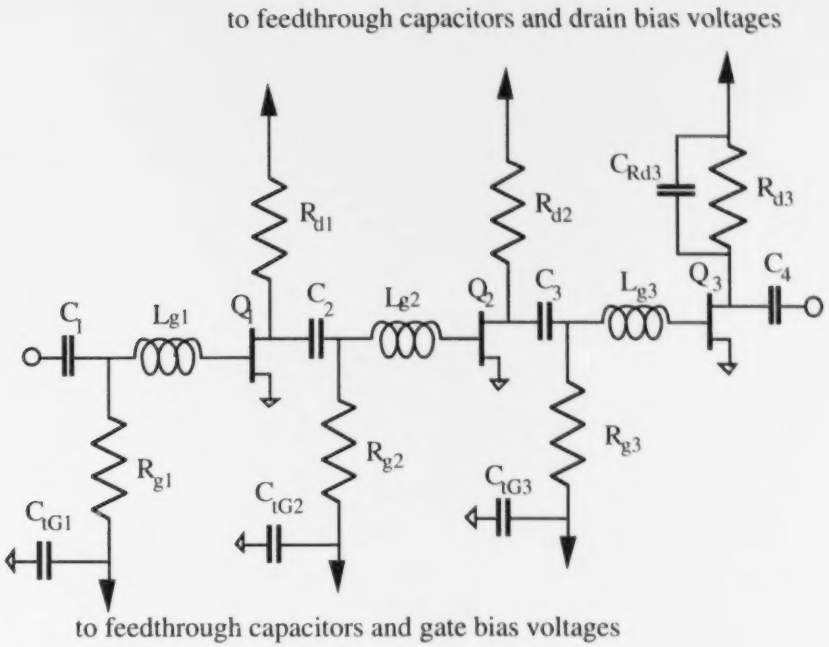


Figure 4.24 Altered amplifier circuit in optical receiver configuration

The resistor values for the circuit of Figure 4.28 are R_{g1} = 34 Ω, R_{g2} = 69 Ω, R_{d3} = 330 Ω, R_{d1} = 33 Ω, R_{d2} = 51 Ω, and R_{d3} = 270Ω. Capacitors C_1, C_2, C_3, and C_4 are all 1.0 nF, and C_{tG1} = 2.2 pF, C_{tG2} = C_{tG3} = 680 pF, and C_{Rd3} = 1.0 pF. All inductances were made to be as close to nominal design values as possible. Bias voltages were adjusted to result in maximum gain, just as they were for the electronic amplifier. These voltages were V_{GG1} = -0.25 V, V_{GG2} = -0.31 V, V_{GG3} = -0.19 V, V_{DD1} = 2.33 V, V_{DD2} = 2.51 V, and V_{DD3} = 5.4 V.

According to [27], at multi-gigahertz frequencies, the output of the MSMs in these linear arrays is position-dependent. That is, the electric signal exiting the array exhibits a spectrum that changes shape as different MSMs in the array are biased and illuminated. When the bias and illumination shifted from the third MSM of the array to the first in the optical receiver, this position dependence became apparent. A slight peak appeared at 5 GHz that was not present in the previous measurement. This response is shown in Figure 4.25.

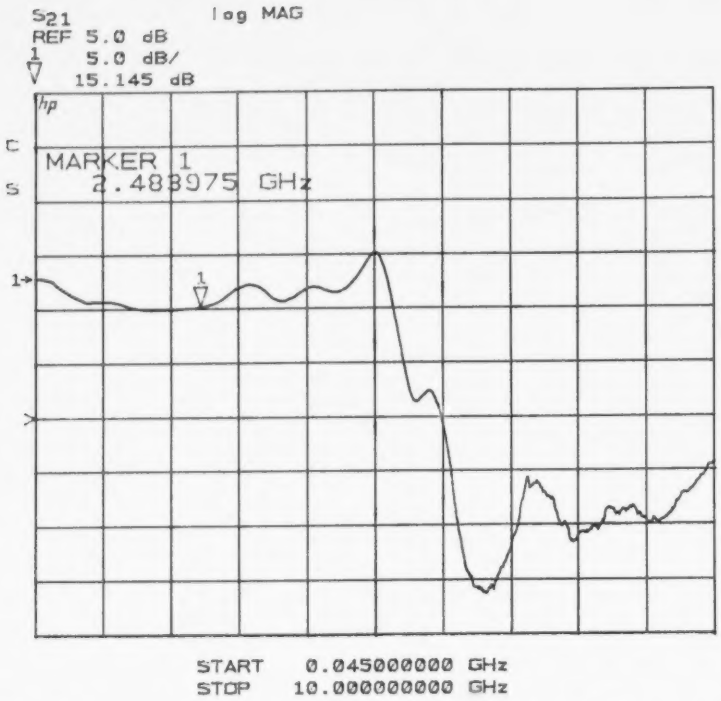


Figure 4.25 Gain spectrum of optical receiver with first MSM illuminated

Finally, a measurement was made using all functioning MSMs in the array. The seventh MSM was shorted and therefore inoperable. By biasing and illuminating each MSM in turn, the seven traces shown in Figure 4.26 were obtained.

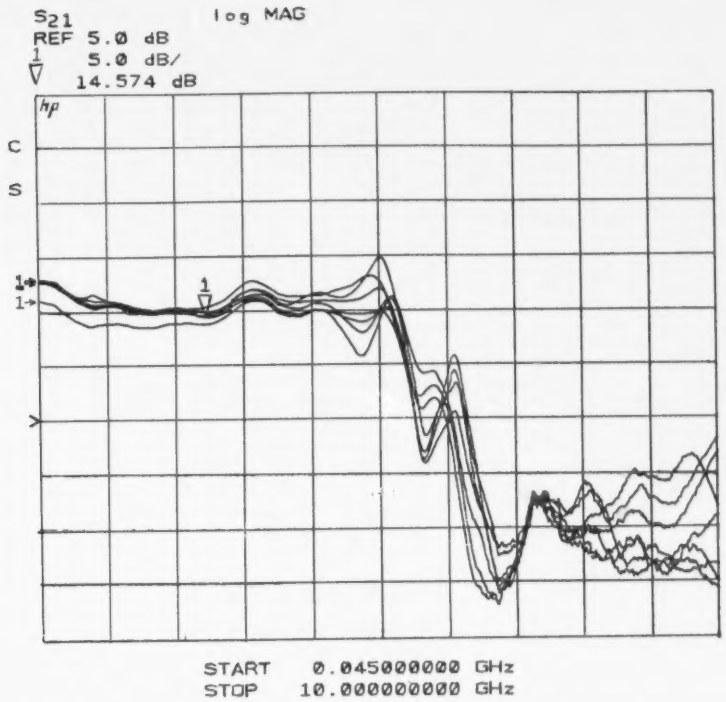


Figure 4.26 Gain spectra of optical receiver with each functioning MSM biased and illuminated one at a time.

The one trace that begins lower than the other six is due to a slight optical fibre-to-MSM misalignment. The two traces with the highest peak and lowest valley in the frequency range 4.7 to 5.0 GHz are produced when the MSMs at the ends of the array are biased and illuminated.

A calculation of transimpedance of the optical receiver can be made using information about the test set-up, the responsivity of the GaAs MSMs in this array, which is 0.2 A/W, and the measured gains of Figure 4.30, where most of the traces exhibit a gain of approximately 15 dB throughout most of their passband. For 0.5 mW of modulated light illuminating a wideband detector having responsivity of 0.13 A/W, the output power at port two of the network analyzer is (0.13 A/W)(0.5 mW) = 0.211 μW = -36.72 dBm, which must then also be the power which is generated at port one, plus the effects of the network analyzer calibration. Now, the same power from port one produces the same 0.5 mW of light shining on an MSM with responsivity of 0.2 A/W, with the output current of (0.5 mW)(0.2 A/W) = 100 μA then fed through a transimpedance amplifier and resulting in a gain of 15 dB as seen at port two of the network analyzer. This results in an output power of -36.72 dBm + 15 dB = -21.75 dBm = 6.68 mW, and an overall MSM-to-optical

receiver output gain of 6.68 mW/100 μA = 66.8 W/A. This corresponds to an output voltage of $\sqrt{(6.68\ \text{mW}/50\ \Omega)} = 11.56$ mV, or a transimpedance of 11.56 mV/100 μA = 115.6 Ω, which is $20\log_{10}(115.6) = 41.3$ dBΩ.

5. Conclusions

An electronic amplifier constructed in hybrid microwave integrated form was designed for a gain of 20 dB and a bandwidth from a few MHz to 6 GHz. In order to achieve these goals, three stages of common-source connected HEMTs were RC coupled together, and peaking inductors were added to the gates of the HEMTs at each stage. This made complicated interstage impedance matching networks unnecessary, and also allowed for the possibility of empirical tuning in the event that the initial measured response did not equal the predicted response.

Upon construction and initial testing, the electronic amplifier did not exhibit a satisfactory result, but after some adjustment, it produced 25.0 dB of gain with about 0.75 dB of ripple up to 5.37 GHz. Input SWR varied from 2 to 4 and output SWR was less than 2.5 in the passband. The phase response was linear, measured noise figure in the passband of 9 to 12 dB agreed well with calculated noise figure, and linear gain was exhibited for output powers up to 2 dBm at 4 GHz.

A second version of this amplifier having a different input transistor had 24.5 dB of gain and a 3 dB-down upper frequency of 5.1 GHz was constructed. This demonstrated the potential of producing the amplifier in small quantities, probably less than ten.

The amplifier was then re-configured to act as an optical receiver. By re-optimizing the amplifier section to perform as a transimpedance amplifier, a set of bias resistor and gate peaking inductor values was determined that resulted in a calculated gain of 50 dBΩ and a bandwidth of 10 GHz. The optical detectors used to achieve this reconfiguration were 1 x 8 linear arrays of GaAs MSM photodetectors.

Again, empirical adjustments to the optical receiver had to be made in order for it to achieve desired performance. After this was done, illuminating one particular MSM in the array with light from an externally-modulated 835 nm laser diode resulted in gain with a ripple of about 3.5 dB up to a frequency of over 5 GHz. Biasing and illuminating each of the seven functioning MSMs in the array in turn showed about 3.5 dB of gain ripple and bandwidths greater than 5 GHz for every MSM acting as a photocurrent source except for the two MSMs at the ends of the array. Each of the PDs located at the ends produced a gain spectrum similar to those of the other five MSMs, except for a 4 dB peak from one and a 4 dB valley from the other at about 4.7 GHz. This arrangement should be able to be used for 10 Gbit/s optoelectronic switching or signal processing.

References

[1] A. Azizi and L. Altwegg, "A 2-GHz Optical Receiver Using Commercially Available Components," Journal of Lightwave Technology, vol. LT-5, no.3, March 1987, pp. 340-343.

[2] Norio Ohkawa, "Fiber-Optic Multigigabit GaAs MIC Front-End Circuit with Inductor Peaking," Journal of Lightwave Technology, vol. 6, no. 11, November 1988, pp. 1665-1671.

[3] James J. Morikuni and Sung-Mo Kang, "An Analysis of Inductive Peaking in Photoreceiver Design," Journal of Lightwave Technology, vol. 10, no. 10, October 1992, pp. 1426-1437.

[4] N. Ohkawa, "20 GHz Bandwidth Low-noise HEMT preamplifier for Optical Receivers," Electronics Letters, 18th August 1988, vol. 24, no. 17, pp. 1061-1062.

[5] Microwave Engineering, by David M. Pozar. Addison-Wesley Publishing Company, Inc., Reading, Massachusetts. 1991, pp. 627-628.

[6] V. Hurm et al., "8.2 GHz Bandwidth Monolithic Integrated Optoelectronic Receiver Using MSM Photodiode and 0.5 µm Recessed-Gate AlGaAs/GaAs HEMTs," Electronics Letters, 25th April 1991, vol. 27, no.9, pp. 734-735

[7] J. S. Wang, C. G. Shih, W. H. Chang, J. R. Middleton, P. J. Apostolakis, and M. Feng, "11 GHz Bandwidth Optical Integrated Receivers Using GaAs MESFET and MSM Technology," IEEE Photonics Technology Letters, vol. 5, no. 3, March 1993, pp. 316-318.

[8] R. I. MacDonald, "Optoelectronic Hybrid Switching," in Photonics in Switching, Volume 1: Background and Components, John E. Midwinter, ed. Academic Press, 1993.

[9] Herbert J. Carlin and James L. Komiak, "A New Method of Broad-Band Equalization Applied to Microwave Amplifier," IEEE Transactions on Microwave Theory and Techniques, vol. MTT-27, no.2, February 1979, pp. 93-99.

[10] Binboga Siddik Yarman and Herbert J. Carlin, "A Simplified 'Real Frequency' Technique Applied to Broad-Band Multistage Microwave Amplifiers," IEEE Transactions on Microwave Theory and Techniques, vol. MTT-30, no. 12, December 1982, pp. 2216-2222.

[11] Kazuhiko Honjo and Yoichihiro Takajama, "GaAs FET Ultrabroad-Band Amplifiers for Gbit/s Data Rate Systems," IEEE Transactions on Microwave Theory and Techniques, vol. MTT-29, no.7, July 1981, pp. 629-636.

[12] A. Perennec, R. Soares, P. Jarry, P. Legaud, and M. Goloubkoff, "Computer-Aided Design of Hybrid and Monolithic Broad-Band Amplifiers for Optoelectronic Receivers," IEEE Transactions on Microwave Theory and Techniques, vol. 37, no.9, September 1989, pp. 1475-1478.

[13] A. Perennec, R. Soares, P. Jarry, P. Legaud, and R. Boittin, "Application of Circuit Synthesis to the Design of a Three-Stage 4 MHz to 7 GHz Amplifier for a Wide Band Fibre

Optics Receiver," presented at the 18th European Microwave Conference, Stockholm, September 1988.

[14] L. D. Tzeng and R. E. Frahm, "Wide Bandwidth Low Noise pinFET Receiver for High-bit-rate Optical Preamplifier Applications," Electronics Letters, 1st September 1988, vol. 24, no. 18, pp. 1132-1134.

[15] M. A. R. Violas, D. J. T. Heatley, A. M. O. Duarte, and D. M. Bedow, "10 GHz Bandwidth Low-noise Optical Receiver Using Discrete Commercial Devices," Electronics Letters, 4th January 1990, vol. 26, no. 1, pp. 35-36.

[16] E. M. Kimber, B. L. Patel, I. Hardcastle and A. Hadjifotiou, "High Performance 10 Gbit/s pin-FET Optical Receiver," Electronics Letters, 16th January 1992, vol. 28, no. 2, pp. 120-122.

[17] N. Ohkawa, J.-I. Yamada, and K. Hagimoto, "Broadband GaAs FET Optical Front-end Circuit up to 5.6 GHz," Electronics Letters, 27th February 1986, vol. 22, no. 5, pp. 259-261.

[18] L. Kasper, J. C. Campbell, J. R. Talman, A. H. Gnauck, J. E. Bowers, and W. S. Holden, "An APD/FET Optical Receiver Operating at 8 Gbit/s," Journal of Lightwave Technology, vol. LT-5, no. 3, March 1987, pp. 344-347.

[19] A. H. Gnauck, C. A. Burrus and D. T. Ekholm, "A Transimpedance APD Optical Receiver Operating at 10 Gb/s," IEEE Photonics Technology Letters, vol. 4, no. 5. May 1992, pp. 468-470.

[20] J. L. Gimlett, "Low-Noise 8 GHz pin/FET Optical Receiver," Electronics Letters, 12th March 1987, vol.23 no. 6, pp. 281-283.

[21] James L. Gimlett, "Ultrawide Bandwidth Optical Receivers," Journal of Lightwave Technology, vol. 7, no. 10, October 1989, pp. 1432-1437.

[22] S. Moustakas and J. L. Hullett, "Noise modelling for broadband amplifier design," IEE Proceedings, vol. 128, pt. G, no. 2, April 1981, pp. 67-76.

[23] Engineering Electronics, A Practical Approach, by Robert Mauro. Prentice Hall, Inc., Englewood Cliffs, New Jersey. 1989. p. 211.

[24] Microwave Engineering, by David M. Pozar. Addison-Wesley Publishing Company, Inc., Reading, Massachusetts. 1991, pp.592-593.

[25] K. Ogawa, "Noise Caused by GaAs MESFETs in Optical Receivers," The Bell System Technical Journal, vol. 60, no. 6, July-August 1981, pp. 923-928.

[26] Sheldon Walklin, private communication

[27] TRLabs Internal Technical Report TR-94-03, R. Sharma, R Tholl, R. DeCorby, and D. Clegg, "Frequency Response Characteristics of GaAs Metal-Semiconductor-Metal (MSM) Photodetector Arrays," April 1994.

Appendix A

Transistor Data Sheets

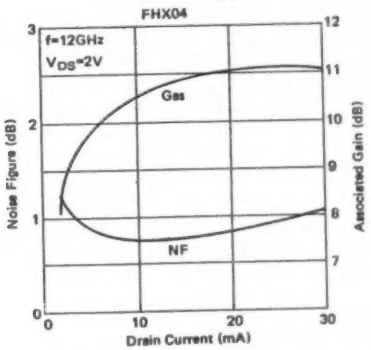
The following four pages contain the transistor data sheets which provided the s-parameters and noise parameters used in the simulation and optimization of the electronic amplifier and the optical receiver. The first two pages are from Fujitsu's catalog for the FHX 04X, 05X, and 06X model HEMTs, and the last two pages were sent along with the FHX 04X and FHX 06X HEMTs that were used in the construction of the electronic amplifier and optical receiver.

FUJITSU **FHX04X FHX05X FHX06X**

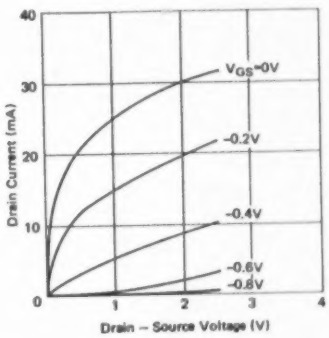
ELECTRICAL CHARACTERISTICS (Ambitnt Temperature Ta = 25°C)

Item		Symbol	Test Conditions	Limit			Unit
				Min.	Typ.	Max.	
Saturation Drain Current		I_{DSS}	V_{DS} = 2V, V_{GS} = 0V	15	30	60	mA
Transconductance		gm	V_{DS} = 2V, I_{DS} = 10mA	35	45	–	mS
Pinch-off Voltage		V_P	V_{DS} = 2V, I_{DS} = 1mA	-0.2	-0.7	-1.5	V
Gate Source Breakdown Voltage		V_{GSO}	I_{GS} = -10μA	-3.0	–	–	V
Noise Figure	FHX04X	NF	V_{DS} = 2V, I_{DS} = 10mA f = 12GHz	–	0.75	0.85	dB
Associated Gain	FHX04X	G_{as}		9.5	10.5	–	dB
Noise Figure	FHX05X	NF		–	0.9	1.1	dB
Associated Gain	FHX05X	G_{as}		9.5	10.5	–	dB
Noise Figure	FHX06X	NF		–	1.1	1.35	dB
Associated Gain	FHX06X	G_{as}		9.5	10.5	–	dB
Small Signal Gain	FHX06X	G_{ss}	Same as above Gain matched	11.0	12.0	–	dB

NF&Gas vs. I_{DS}



DRAIN CURRENT vs. DRAIN-SOURCE VOLTAGE

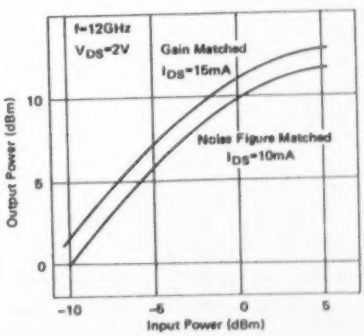


NOISE PARAMETERS

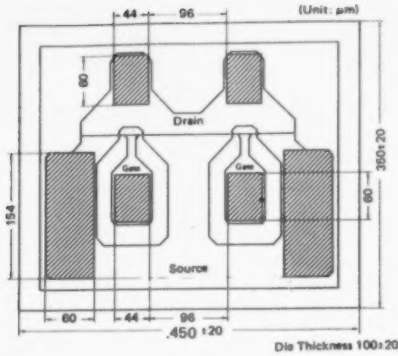
V_{DS} = 2 V, I_{DS} = 10 mA

Freq. (GHz)	Γopt		NFmin (dB)	Rn/50
	MAG	ANG		
2	.790	16.0	.33	.500
4	.730	49.0	.35	.450
6	.670	85.0	.45	.310
8	.600	114.0	.55	.190
10	.520	134.0	.66	.140
12	.450	160.0	.75	.100
14	.400	-174.0	.88	.100
16	.340	-148.0	1.15	.090
18	.260	-122.0	1.30	.090

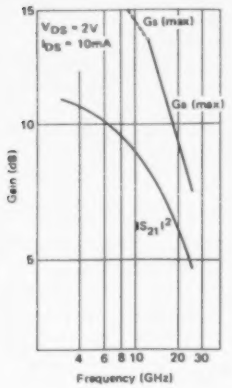
OUTPUT POWER vs. INPUT POWER



CHIP OUTLINE



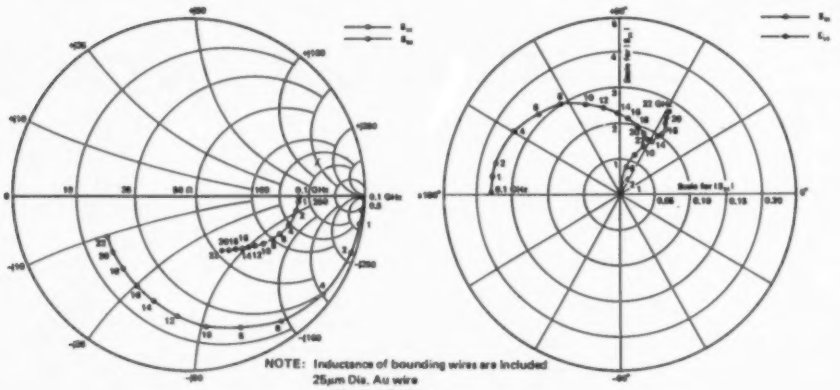
Ga (max) & $|S_{21}|^2$ vs. FREQUENCY



S-PARAMETERS

V_{DS} = 2V, I_{DS} = 10mA

FREQ.	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100	1.000	-.9	3.721	179.2	.001	89.5	.606	-.4
500	.999	-4.7	3.717	176.0	.007	87.7	.605	-2.1
1000	.996	-9.5	3.705	172.0	.013	85.4	.604	-4.2
2000	.983	-18.8	3.658	164.1	.026	81.0	.596	-8.3
3000	.964	-28.0	3.585	156.4	.038	76.7	.588	-12.3
4000	.938	-37.0	3.489	149.0	.049	72.8	.576	-16.0
5000	.909	-45.6	3.377	141.9	.059	69.2	.562	-19.6
6000	.877	-54.0	3.255	135.1	.068	66.0	.547	-22.9
7000	.844	-62.1	3.128	128.6	.076	63.2	.531	-26.0
8000	.811	-69.8	2.999	122.5	.082	60.8	.516	-28.9
9000	.779	-77.3	2.873	166.7	.088	58.8	.500	-31.7
10000	.748	-84.5	2.750	111.2	.093	57.3	.485	-34.2
11000	.720	-91.5	2.633	106.1	.097	56.1	.471	-36.7
12000	.694	-98.2	2.521	101.1	.101	55.2	.457	-39.1
13000	.670	-104.7	2.417	96.5	.105	54.8	.444	-41.4
14000	.649	-111.1	2.319	92.0	.108	54.6	.432	-43.7
15000	.630	-117.2	2.227	87.7	.111	54.6	.421	-46.0
16000	.614	-123.2	2.142	83.6	.114	55.0	.410	-48.4
17000	.600	-129.0	2.062	79.7	.118	55.5	.400	-50.7
18000	.588	-134.6	1.988	75.9	.121	56.2	.391	-53.2
19000	.578	-140.1	1.918	72.3	.125	57.0	.382	-55.7
20000	.570	-145.4	1.853	68.8	.130	57.8	.373	-58.4
21000	.564	-150.6	1.793	65.4	.134	58.7	.365	-61.1
22000	.560	-155.6	1.736	62.1	.140	59.6	.358	-64.0



NOTE: Inductance of bounding wires are included
25μm Dia. Au wire
n : Number of wires
Gate n = 2 (Length = 0.3 mm)
Drain n = 2 (Length = 0.3 mm)
Source n = 4 (Length = 0.3 mm)

GaAs FET Pilot Test Data FUJITSU LIMITED

TYPE NO. FHX04X LOT NO. HCE 8- 4 · TEST DATE 91.01.14

ITEM	DC TEST				RF TEST			
	VGSO	IDSS	gm	VP	NF	Gas		
UNIT	V	mA	mS	V	dB	dB		
TEST CONDITIONS	IGS= -10 μA	VDS= 2 V VGS= 0 V	VDS= 2 V IDS= 10 mA	VDS= 2 V IDS= 1 mA	VDS= 2 V IDS=10 mA f = 12 GHz			
1	- 7.3	23.1	50.4	-0.47	0.76	11.86		
2	- 7.6	23.1	50.2	-0.47	0.79	11.85		
3	- 6.6	29.9	51.6	-0.59	0.82	11.80		
4	- 6.6	33.2	50.4	-0.69	0.75	11.87		
5	- 6.9	28.6	49.6	-0.59	0.81	12.18		
6	- 7.4	23.3	51.2	-0.47	0.76	12.19		
7	- 7.0	26.6	47.2	-0.59	0.76	11.68		
8	- 6.3	34.1	50.0	-0.71	0.80	11.58		
9	- 7.6	24.8	49.0	-0.51	0.75	12.15		
10	- 7.5	24.2	52.6	-0.48	0.76	11.95		
LIMIT	> - 3	15 ~ 60	> 35	-0.2~-1.5	< 0.85	> 9.5		

DC Parameter : Sample size 10 Pcs , Criteria (accept,reject) = (0,1)
RF Parameter : Sample size 10 Pcs , Criteria (accept,reject) = (2,3)

Approval: H Togashi

GaAs FET Pilot Test Data　　FUJITSU LIMITED

TYPE NO. FHX06X　　LOT NO. HCS136-05　　TEST DATE 93.02.17

ITEM	DC TEST				RF TEST			
	VGSO	IDSS	gm	VP	NF	Gas		
UNIT	V	mA	mS	V	dB	dB		
TEST CONDITIONS	IGS= -10 μA	VDS= 2 V VGS= 0 V	VDS= 2 V IDS= 10 mA	VDS= 2 V IDS= 1 mA	VDS= 2 V IDS=10 mA f = 12 GHz			
1	- 4.4	32.4	60.8	-0.61	0.61	12.39		
2	- 5.1	27.6	62.0	-0.49	0.63	12.78		
3	- 5.0	31.4	61.4	-0.50	0.64	12.25		
4	- 6.9	31.9	61.4	-0.51	0.64	11.61		
5	- 5.5	33.1	57.8	-0.58	0.67	13.16		
6	- 6.8	31.8	61.8	-0.51	0.64	11.96		
7	- 4.8	34.0	59.4	-0.56	0.64	12.15		
8	- 5.6	33.1	58.0	-0.58	0.65	12.58		
9	- 5.0	31.1	61.6	-0.50	0.62	12.59		
10	- 5.2	30.1	61.6	-0.49	0.64	12.90		
LIMIT	> - 3	15 ~ 60	> 35	-0.2~-1.5	< 1.35	> 9.5		

DC Parameter : Sample size 10 Pcs , Criteria (accept,reject) = (0,1)
RF Parameter : Sample size 10 Pcs , Criteria (accept,reject) = (2,3)

Approval: T. Togashi

Appendix B

Bond Wire Inductance Calculations

In order to take advantage of inductive peaking techniques, a way had to be found to design and construct inductances on the order of a few nanohenrys. This was accomplished by using parallel pairs of 1.25-mil diameter, 99.99% gold bond wires of appropriate length, wedge-bonded into place. Three different ways were found to calculate how much inductance is produced by a given length of a bond wire pair.

First, from E. D. Ostroff et al., "Solid State Radar Transmitters," Artech House Inc., 1985, pp. 63-64, for the wire profile shown in Figure B.1, the equivalent inductance of parallel wires can be calculated as

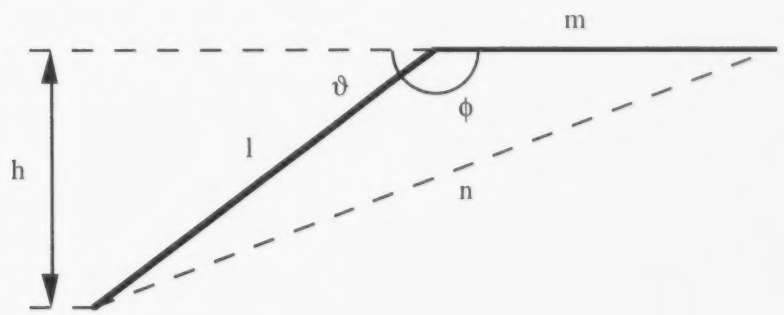


Figure B.1 Wire profile for equivalent inductance calculation

$$L_{equiv} = \frac{L_{int} + L_{ext} + L_p + 2L_m}{\text{number of wires}}$$

where

- L_{int} is internal inductance of a wire of circular cross section as a function of radius and frequency

$$L_{int} = \frac{\mu_0 l}{4\pi} \frac{\delta}{a}$$

- L_{ext} is the inductance of a wire of circular cross section as a function of radius and length

$$L_{ext} = \frac{\mu_0 l}{4\pi}\left[\ln\left(\frac{l}{a} + \sqrt{1+\left(\frac{l}{a}\right)^2}\right) - \sqrt{1+\left(\frac{a}{l}\right)^2} + \frac{a}{l}\right]$$

- L_p is a measure of the mutual inductance due to parallel wires of length l separated by spacing s

$$L_p = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l}{s}+\sqrt{1+\left(\frac{l}{s}\right)^2}\right)-\sqrt{1+\left(\frac{a}{l}\right)^2}+\frac{s}{l}\right]$$

- L_m is a measure of the mutual inductance that occurs between two segments of the same wire offset by angle ϑ

$$L_m = \frac{\mu_0}{2\pi}\cos\theta\left[l\tanh^{-1}\left(\frac{m}{l+n}\right)+m\tanh^{-1}\left(\frac{l}{m+n}\right)\right]$$

where

- l, m = lengths of wire segments, as in above figure
- a = radius of wire
- s = spacing between wires
- μ_0 = magnetic permeability of free space = 4π x 10^{-7} H/m
- $\phi = \cos^{-1}\left(\frac{h}{l}\right)+\frac{\pi}{2}$
- $n = \sqrt{l^2+m^2-2lm\cos\phi}$
- skin depth, $\delta = \frac{1}{\sqrt{\pi f\mu\sigma}}$

  where

  - f is frequency in Hz
  - μ is the magnetic permeability of the wire, and
  - σ is the conductivity of the wire.

This simplifies due to the fact that L_{ext} and L_p are much larger terms than L_{int} and L_m, so L_{equiv} now becomes

$$L_{equiv} \cong \frac{L_{ext}+L_p}{\text{number of wires}}.$$

L_{equiv} is now independent of frequency, and of the angle and position of the bend in the wire(s).

Alternatively, from Allen A. Sweet, "MIC and MMIC Amplifier and Oscillator Circuit Design," Artech House Inc., p. 229, the inductance of a bond wire in free space is given as

$$L = 2l\left[\ln\left(\frac{l}{d}\right)+0.5+0.22\left(\frac{2d}{l}\right)\right] \text{ nH}$$

where l is wire length, in cm, and d is wire diameter, in cm.

The mutual inductance between two parallel bond wires in free space, separated by a distance s (in cm), is given as

$$L = 2l\left[\ln\left(\frac{l}{s}\right) - 1.0 + \frac{s}{l} - 0.25\left(\frac{s}{l}\right)^2\right] \quad \text{nH}$$

where again, l is wire length in cm.

Calculations of bond wire inductance based on each set of equations were carried out, for wire lengths from 150 μm to 4000 μm and from 10 μm to 500 μm, and for number of wires = 2, 3, 4, 5, and 6. Both Ostroff's and Sweet's equations give curves of the same shape, but Sweet's values are consistently lower than Ostroff's by about 8%. This is illustrated in Figure B.2.

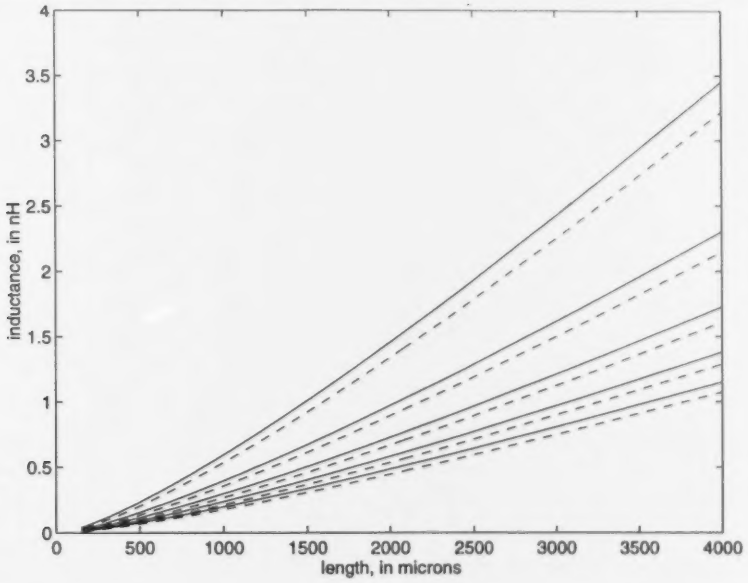


Figure B.2 Comparing Ostroff's (solid) and Sweet's (dashed) bond wire inductance values, for wire lengths from 150 to 4000 μm

Using HP's MDS, it was possible to determine the value of an ideal inductance with the same s-parameters as a pair of WIRES (wire over substrate) components defined as 1.25 mil diameter, 99.99% gold bond wires. The results of this work are shown in Figure B.3. This calculation confirmed the approximate validity of Ostroff's and Sweet's equations for inductance values less than about 0.4 nH, or bond wire pair lengths of less than about 1000 μm, but not for longer wires.

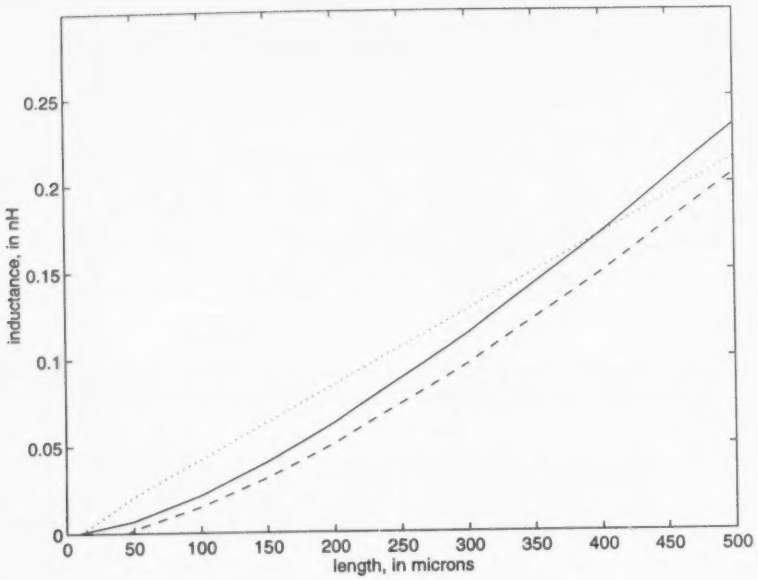


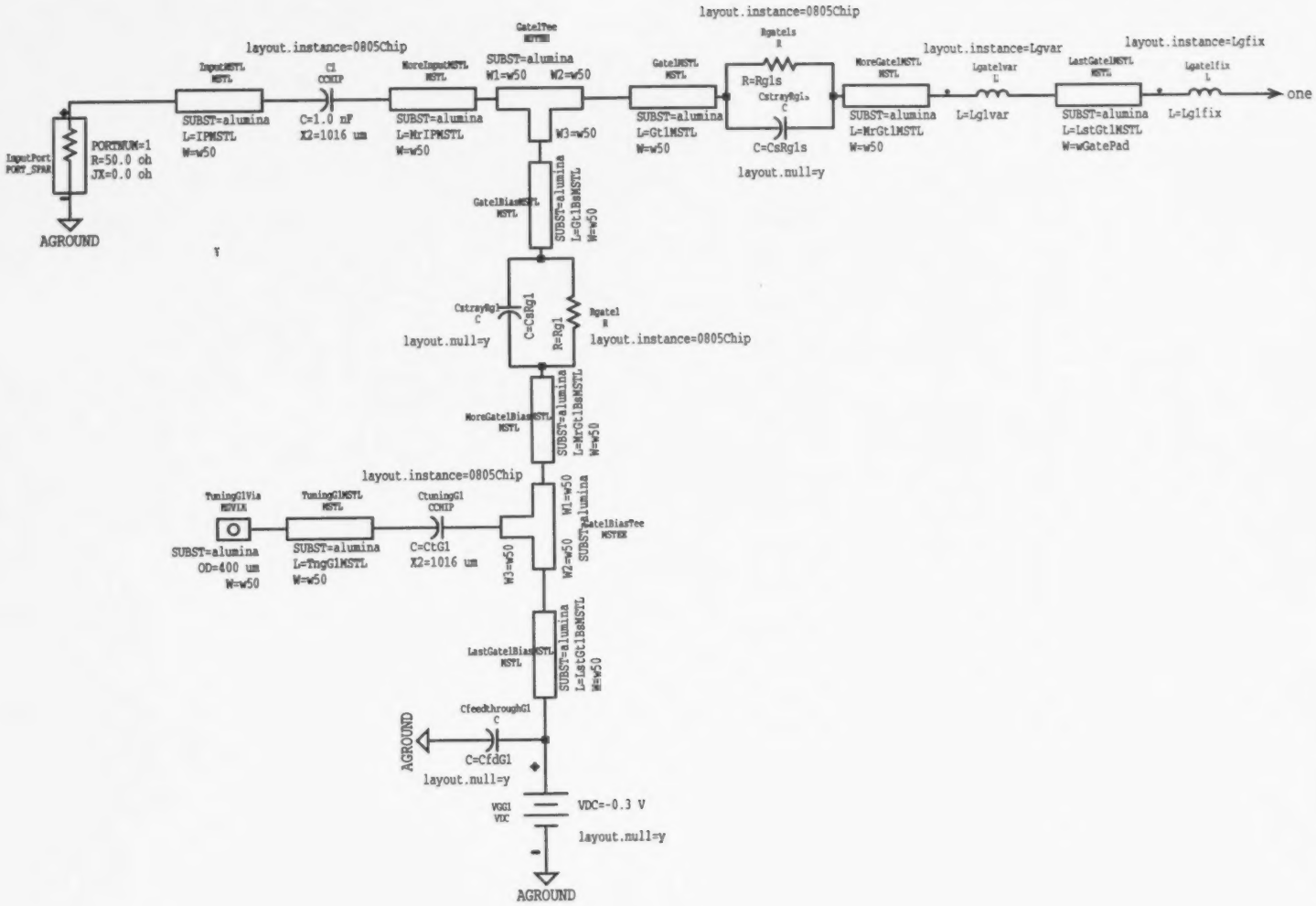
Figure B.3 Comparing bond wire inductance calculations using MDS (dotted) with Ostroff's (solid) and Sweet's (dashed) calculations

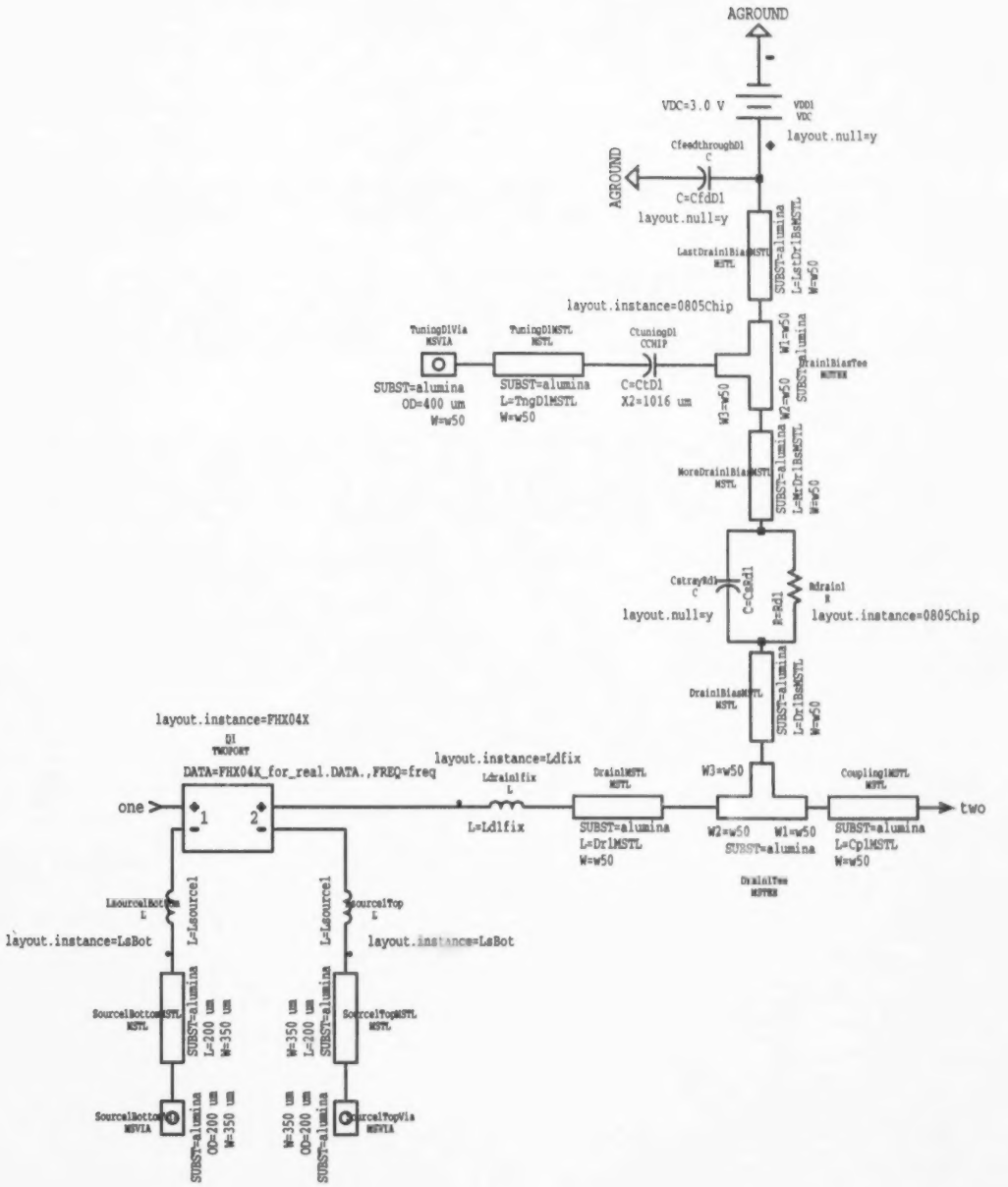
It was decided to use a mean value between Ostroff's and Sweet's calculations to guide the construction of gate peaking inductors. Both sets of curves have the same shape, and differ by only about 8%.

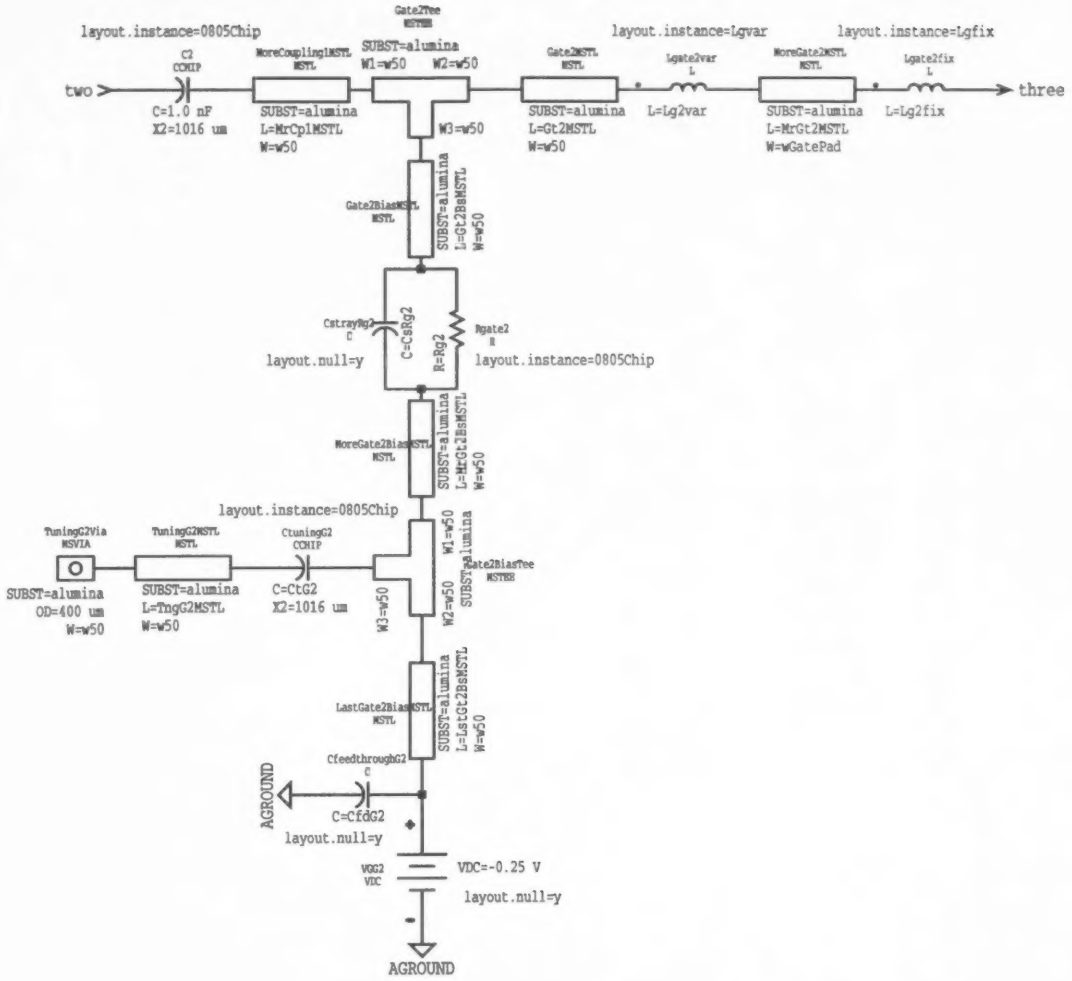
Appendix C

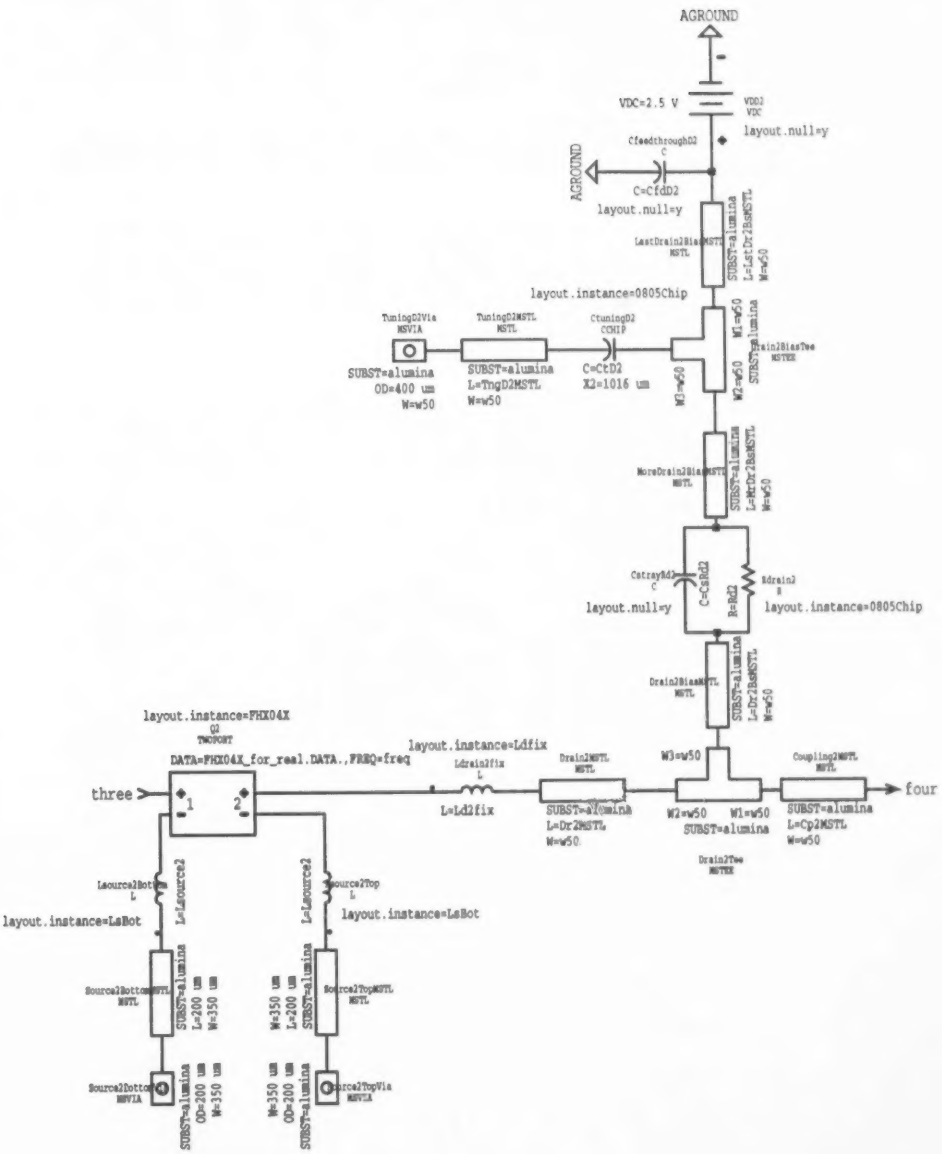
MDS Design Files of Electronic Amplifier

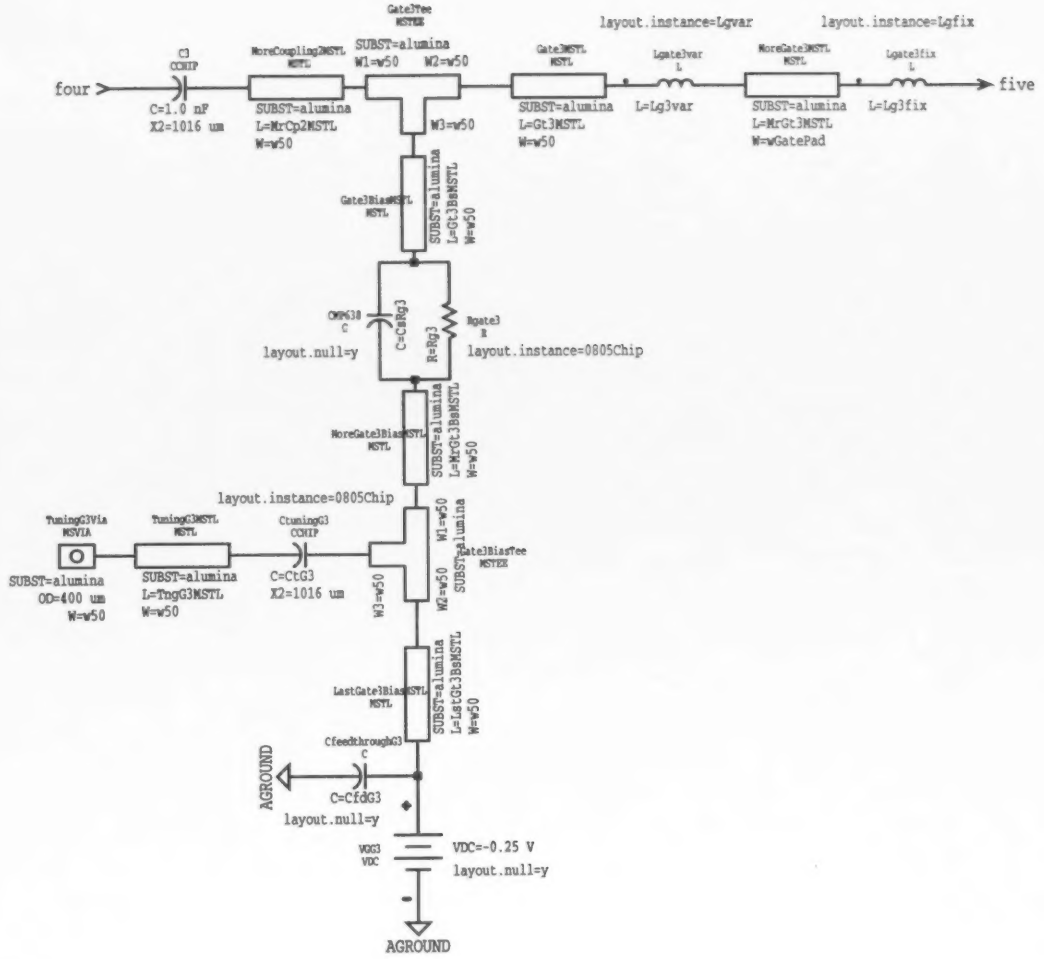
The following seven pages contain the complete circuit file used to design and optimize the electronic amplifier for 20 dB of gain up to 6 GHz and 17.5 dB of gain up to 7 GHz. The two s-parameter 50 Ω ports were removed and replaced with an AC current source at the input and a 50 Ω resistor at the output to form a transimpedance amplifier, and was subsequently optimized to provide 50 dBΩ of gain up to 10 GHz for use as an optical receiver.

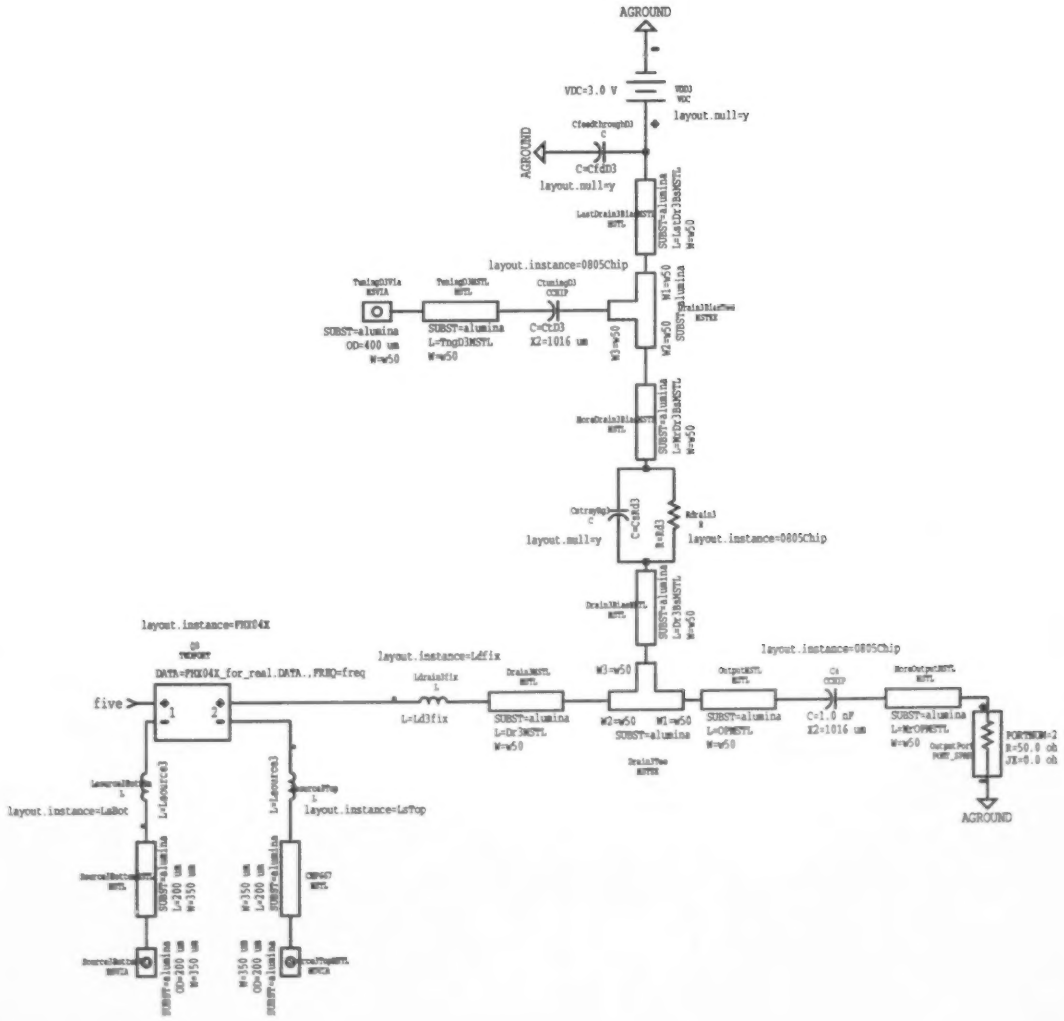

layout.instance=0805Chip
InputMSTL
MSTL
SUBST=alumina
L=IPMSTL
W=w50
C1
CCHIP
C=1.0 nF
X2=1016 um
MoreInputMSTL
MSTL
SUBST=alumina
L=MrIPMSTL
W=w50
GatelTee
MSTEE
SUBST=alumina
W1=w50
W2=w50
W3=w50
GatelMSTL
MSTL
SUBST=alumina
L=Gt1MSTL
W=w50
Rgatels
R
R=Rg1s
CstrayRg1s
C
C=CsRg1s
layout.null=y
MoreGatelMSTL
MSTL
SUBST=alumina
L=MrGt1MSTL
W=w50
layout.instance=Lgvar
Lgatelvar
L
L=Lg1var
LastGatelMSTL
MSTL
SUBST=alumina
L=LstGt1MSTL
W=wGatePad
layout.instance=Lgfix
Lgatelfix
L
L=Lg1fix
one
InputPort
PORT_SPAR
PORTNUM=1
R=50.0 oh
JX=0.0 oh
AGROUND
GatelBiasMSTL
MSTL
SUBST=alumina
L=Gt1BiMSTL
W=w50
CstrayRg1
C
C=CsRg1
Rgatel
R
R=Rg1
layout.null=y
layout.instance=0805Chip
MoreGatelBiasMSTL
MSTL
SUBST=alumina
L=MrGt1BiMSTL
W=w50
layout.instance=0805Chip
TuningG1Via
MSVIA
SUBST=alumina
OD=400 um
W=w50
TuningG1MSTL
MSTL
SUBST=alumina
L=TngG1MSTL
W=w50
CtuningG1
CCHIP
C=CtG1
X2=1016 um
W1=w50
W2=w50
W3=w50
GatelBiasTee
MSTEE
SUBST=alumina
LastGatelBiasMSTL
MSTL
SUBST=alumina
L=LstGt1BiMSTL
W=w50
CfeedthroughG1
C
C=CfdG1
AGROUND
layout.null=y
VGG1
VDC
VDC=-0.3 V
layout.null=y
AGROUND


AGROUND
VDC=3.0 V
VDD1
VDC
layout.null=y
CfeedthroughD1
C
AGROUND
C=CfdD1
layout.null=y
LastDrainlBiasMSTL
MSTL
SUBST=alumina
L=LstDr1BsMSTL
W=w50
layout.instance=0805Chip
TuningD1Via
MSVIA
TuningD1MSTL
MSTL
CtuningD1
CCHIP
SUBST=alumina
OD=400 um
W=w50
SUBST=alumina
L=TngD1MSTL
W=w50
C=CtD1
X2=1016 um
W1=w50
W2=w50
W3=w50
SUBST=alumina
DrainlBiasTee
MSTEE
MoreDrainlBiasMSTL
MSTL
SUBST=alumina
L=MrDr1BsMSTL
W=w50
CstrayRd1
C
C=CsRd1
Rdrain1
R
R=Rd1
layout.null=y
layout.instance=0805Chip
DrainlBiasMSTL
MSTL
SUBST=alumina
L=Dr1BsMSTL
W=w50
layout.instance=FHX04X
DI
TWOPORT
DATA=FHX04X_for_real.DATA.,FREQ=freq
layout.instance=Ldfix
LdrainlfixL
L
DrainlMSTL
MSTL
W3=w50
CouplingIMSTL
MSTL
one
two
1
2
L=Ld1fix
SUBST=alumina
L=Dr1MSTL
W=w50
W2=w50
W1=w50
SUBST=alumina
DrainlTee
MSTEE
SUBST=alumina
L=CplMSTL
W=w50
LsourcelBottom
L
L=Lsource1
LsourcelTop
L
L=Lsource1
layout.instance=LsBot
layout.instance=LsBot
SourcelBottomMSTL
MSTL
SUBST=alumina
L=200 um
W=350 um
SourcelTopMSTL
MSTL
W=350 um
L=200 um
SUBST=alumina
SourcelBottomVia
MSVIA
SUBST=alumina
OD=200 um
W=350 um
SourcelTopVia
MSVIA
W=350 um
OD=200 um
SUBST=alumina


layout.instance=0805Chip
Gate2Tee
MSTEE
SUBST=alumina
W1=w50
W2=w50
layout.instance=Lgvar
layout.instance=Lgfix
C2
CCHIP
MoreCoupling1MSTL
MSTL
Gate2MSTL
MSTL
Lgate2var
L
MoreGate2MSTL
MSTL
Lgate2fix
L
two
three
C=1.0 nF
X2=1016 um
SUBST=alumina
L=MrCp1MSTL
W=w50
W3=w50
SUBST=alumina
L=Gt2MSTL
W=w50
L=Lg2var
SUBST=alumina
L=MrGt2MSTL
W=wGatePad
L=Lg2fix
Gate2BiasMSTL
MSTL
SUBST=alumina
L=Gt2BsMSTL
W=w50
CstrayRg2
C
C=CsRg2
Rgate2
R
R=Rg2
layout.null=y
layout.instance=0805Chip
MoreGate2BiasMSTL
MSTL
SUBST=alumina
L=MrGt2BsMSTL
W=w50
layout.instance=0805Chip
TuningG2Via
MSVIA
TuningG2MSTL
MSTL
CtuningG2
CCHIP
SUBST=alumina
OD=400 um
W=w50
SUBST=alumina
L=TngG2MSTL
W=w50
C=CtG2
X2=1016 um
W3=w50
W1=w50
W2=w50
SUBST=alumina
Gate2BiasTee
MSTEE
LastGate2BiasMSTL
MSTL
SUBST=alumina
L=LstGt2BsMSTL
W=w50
CfeedthroughG2
C
AGROUND
C=CfdG2
layout.null=y
VGG2
VDC
VDC=-0.25 V
layout.null=y
AGROUND

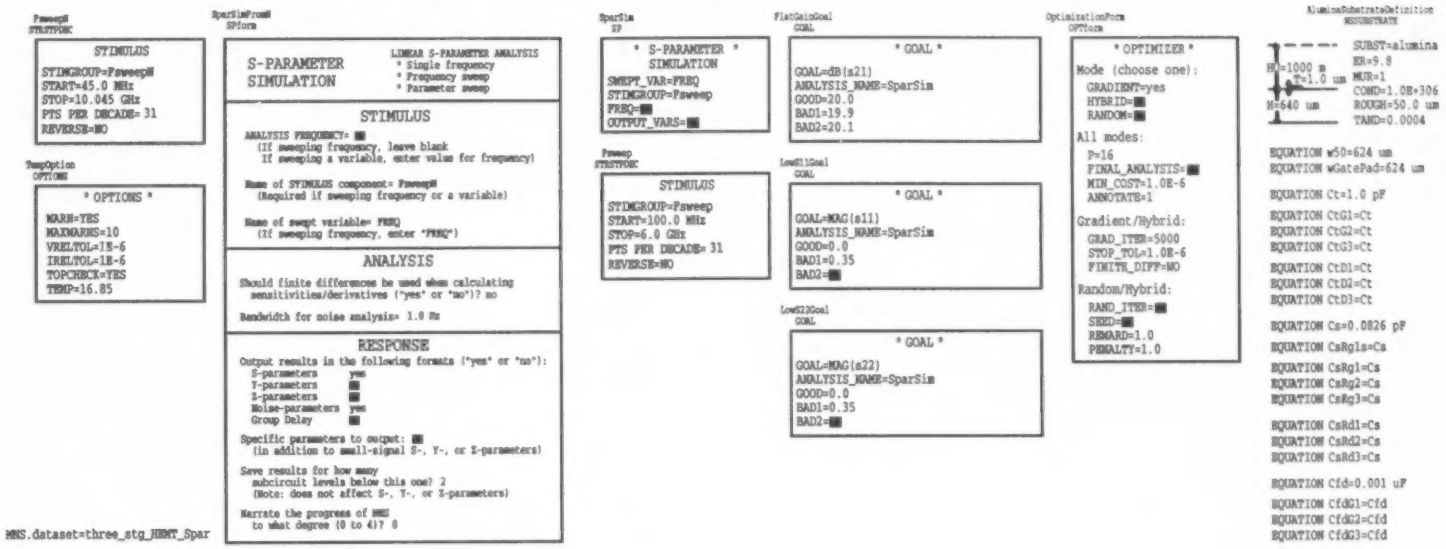

AGROUND
VDC=2.5 V
VDD2
VDC
layout.null=y
CfeedthroughD2
C
AGROUND
C=CfdD2
layout.null=y
LastDrain2BiasMSTL
MSTL
SUBST=alumina
L=LstDr2BsMSTL
W=w50
layout.instance=0805Chip
TuningD2Via
MSVIA
TuningD2MSTL
MSTL
CtuningD2
CCHIP
SUBST=alumina
OD=400 um
W=w50
SUBST=alumina
L=TngD2MSTL
W=w50
C=CtD2
X2=1016 um
W3=w50
W1=w50
W2=w50
SUBST=alumina
Drain2BiasTee
MSTEE
MoreDrain2BiasMSTL
MSTL
SUBST=alumina
L=MrDr2BsMSTL
W=w50
CstrayD2
C
C=CdrD2
Rdrain2
R
R=Rd2
layout.null=y
layout.instance=0805Chip
Drain2BiasMSTL
MSTL
SUBST=alumina
L=Dr2BsMSTL
W=w50
layout.instance=FHX04X
Q2
TWOPORT
DATA=FHX04X_for_real.DATA.,FREQ=freq
three
four
1
2
layout.instance=Ldfix
Ldrain2fix
L
L=Ld2fix
Drain2MSTL
MSTL
SUBST=alumina
L=Dr2MSTL
W=w50
W3=w50
W2=w50
W1=w50
SUBST=alumina
Drain2Tee
MSTEE
Coupling2MSTL
MSTL
SUBST=alumina
L=Cp2MSTL
W=w50
Lsource2Bottom
L
Lsource2
Lsource2Top
L
layout.instance=LsBot
layout.instance=LsBot
Source2BottomMSTL
MSTL
SUBST=alumina
L=200 um
W=350 um
Source2TopMSTL
MSTL
W=350 um
L=200 um
SUBST=alumina
Source2BottomVia
MSVIA
SUBST=alumina
OD=200 um
W=350 um
Source2TopVia
MSVIA
W=350 um
OD=200 um
SUBST=alumina


four
five
C1
CCHIP
C=1.0 nF
X2=1016 um
MoreCoupling2MSTL
MSTL
SUBST=alumina
L=MrCp2MSTL
W=w50
Gate3Tee
MSTEE
SUBST=alumina
W1=w50
W2=w50
W3=w50
Gate3MSTL
MSTL
SUBST=alumina
L=Gt3MSTL
W=w50
layout.instance=Lgvar
Lgate3var
L
L=Lg3var
layout.instance=Lgfix
MoreGate3MSTL
MSTL
SUBST=alumina
L=MrGt3MSTL
W=wGatePad
Lgate3fix
L
L=Lg3fix
Gate3BiasMSTL
MSTL
SUBST=alumina
L=Gt3BiaMSTL
W=w50
CMPG30
C
C=CdRg3
Rgate3
R
R=Rg3
layout.null=y
layout.instance=0805Chip
MoreGate3BiasMSTL
MSTL
SUBST=alumina
L=MrGt3BiaMSTL
W=w50
layout.instance=0805Chip
TuningG3Via
MSVIA
SUBST=alumina
OD=400 um
W=w50
TuningG3MSTL
MSTL
SUBST=alumina
L=TngG3MSTL
W=w50
CtuningG3
CCHIP
C=CtG3
X2=1016 um
W1=w50
W2=w50
W3=w50
Gate3BiasTee
MSTEE
SUBST=alumina
LastGate3BiasMSTL
MSTL
SUBST=alumina
L=LstGt3BiaMSTL
W=w50
CfeedthroughG3
C
C=CfdG3
layout.null=y
AGROUND
VGG3
VDC
VDC=-0.25 V
layout.null=y
AGROUND


AGROUND
VDC=3.0 V
VDD3
VDC
layout.null=y
CfeedthroughD3
C
AGROUND
C=CfdD3
layout.null=y
LastDrain3BlaMSTL
MSTL
SUBST=alumina
L=LaDr3BkMSTL
W=w50
layout.instance=0805Chip
TwinqD1Via
MSVIA
TwinqD1MSTL
MSTL
CtuningD3
CCHIP
SUBST=alumina
OD=400 um
W=w50
SUBST=alumina
L=TngD1MSTL
W=w50
C=CtD3
X2=1016 um
W1=w50
W2=w50
W3=w50
SUBST=alumina
DrainBlaTwo
MSTEX
MoreDrain3BlaMSTL
MSTL
SUBST=alumina
L=MrDr3BkMSTL
W=w50
CntrayDp3
C
C=CBd3
R=Rd3
layout.null=y
Rdrain3
R
layout.instance=0805Chip
DrainBkLasMSTL
MSTL
SUBST=alumina
L=Dr3BkMSTL
W=w50
layout.instance=FHX04X
S2
TWOPORT
DATA=FHX04X_for_real.DATA.,FREQ=freq
layout.instance=Ldfix
LdrainDfix
L
L=Ld3fix
DrainMSTL
MSTL
SUBST=alumina
L=Dr3MSTL
W=w50
W1=w50
W2=w50
W1=w50
SUBST=alumina
DrainTwo
MSTEX
layout.instance=0805Chip
OutputMSTL
MSTL
SUBST=alumina
L=OPMSTL
W=w50
C4
CCHIP
C=1.0 nF
X2=1016 um
MoreOutputMSTL
MSTL
SUBST=alumina
L=MrOPMSTL
W=w50
OutputPort
PORT_DBWV
PORTNUM=2
R=50.0 oh
JX=0.0 oh
AGROUND
five
1
2
LsourceBotMSTL
L
L=Lsource3
layout.instance=LsBot
LsourceTopMSTL
L
L=Lsource3
layout.instance=LsTop
SourceBotMSTL
MSTL
SUBST=alumina
L=200 um
W=350
SourceBotViaMSTL
MSVIA
SUBST=alumina
OD=200 um
W=350
CBP467
MSTL
SUBST=alumina
W=350 um
L=200 um
SourceTopMSTL
MSVIA
SUBST=alumina
W=350 um
OD=300 um

These s-parameter simulation blocks are for NOISE ANALYSIS.

These s-parameter simulation blocks are for OPTIMIZATION.




```
EQUATION w50=624 um
EQUATION wGatePad=624 um

EQUATION Ct=1.0 pF

EQUATION CtG1=Ct
EQUATION CtG2=Ct
EQUATION CtG3=Ct

EQUATION CtD1=Ct
EQUATION CtD2=Ct
EQUATION CtD3=Ct

EQUATION Cs=0.0826 pF

EQUATION CsRg1s=Cs

EQUATION CsRg1=Cs
EQUATION CsRg2=Cs
EQUATION CsRg3=Cs

EQUATION CsRd1=Cs
EQUATION CsRd2=Cs
EQUATION CsRd3=Cs

EQUATION Cfd=0.001 uF

EQUATION CfdG1=Cfd
EQUATION CfdG2=Cfd
EQUATION CfdG3=Cfd

EQUATION CfdD1=Cfd
EQUATION CfdD2=Cfd
EQUATION CfdD3=Cfd
```

```
EQUATION Lg1var=(0.20<0.96<2.50) nH
EQUATION Lg2var=(0.20<1.97<2.50) nH
EQUATION Lg3var=(0.20<0.24<2.50) nH

EQUATION Lg1fix = 0.0 nH
EQUATION Lg2fix = 0.0 nH
EQUATION Lg3fix = 0.0 nH

EQUATION Ld1fix = 0.0 nH
EQUATION Ld2fix = 0.0 nH
EQUATION Ld3fix = 0.0 nH
```

```
EQUATION Lsource=0.15 nH

EQUATION Lsource1=Lsource
EQUATION Lsource2=Lsource
EQUATION Lsource3=Lsource
```

```
EQUATION IPMSTL=4146 um
EQUATION MrIPMSTL=1662 um
EQUATION Gt1BsMSTL=1350 um
EQUATION MrGt1BsMSTL=1887 um
EQUATION TngG1MSTL=900 um
EQUATION LstGt1BsMSTL=1985 um
EQUATION Gt1MSTL=1662 um
EQUATION MrGt1MSTL=1108 um
EQUATION LstGt1MSTL=125 um
EQUATION Dr1MSTL=612 um
EQUATION Dr1BsMSTL=1350 um
EQUATION MrDr1BsMSTL=1887 um
EQUATION TngD1MSTL=900 um
EQUATION LstDr1BsMSTL=1985 um
EQUATION Cp1MSTL=1662 um
EQUATION MrCp1MSTL=1662 um
```

```
EQUATION Gt2BsMSTL=1350 um
EQUATION MrGt2BsMSTL=1887 um
EQUATION TngG2MSTL=900 um
EQUATION LstGt2BsMSTL=1985 um
EQUATION Gt2MSTL=437 um
EQUATION MrGt2MSTL=125 um

EQUATION Dr2MSTL=612 um
EQUATION Dr2BsMSTL=1350 um
EQUATION MrDr2BsMSTL=1887 um
EQUATION TngD2MSTL=900 um
EQUATION LstDr2BsMSTL=1985 um
EQUATION Cp2MSTL=1662 um
EQUATION MrCp2MSTL=1662 um
```

```
EQUATION Gt3BsMSTL=1350 um
EQUATION MrGt3BsMSTL=1887 um
EQUATION TngG3MSTL=900 um
EQUATION LstGt3BsMSTL=1985 um
EQUATION Gt3MSTL=437 um
EQUATION MrGt3MSTL=125 um

EQUATION Dr3MSTL=612 um
EQUATION Dr3BsMSTL=1350 um
EQUATION MrDr3BsMSTL=1887 um
EQUATION TngD3MSTL=900 um
EQUATION LstDr3BsMSTL=1985 um

EQUATION OPMSTL=1662 um
EQUATION MrOPMSTL=4147 um
```

```
EQUATION Rg1s=(10.0<147.7<680.0) oh

EQUATION Rg1=(10.0<184.3<680.0) oh
EQUATION Rg2=(10.0<680.0<680.0) oh
EQUATION Rg3=(10.0<187.9<680.0) oh

EQUATION Rd1=(10.0<66.5<680.0) oh
EQUATION Rd2=(10.0<39.3<680.0) oh
EQUATION Rd3=(10.0<680.0<680.0) oh
```

Appendix D

Matlab Files Used to Generate Eye Diagram

The following three Matlab files were used in the generation of the eye diagram shown in Figure 4.24. The first listing is "eye_gen.m", and is the main program which contains the amplifier frequency response through which is sent a random 10 Gbit/s signal. The second listing is the function "show_eyeB.m", which takes the time domain representation of the 10 Gbit/s signal coming out of the amplifier and generated an eye diagram with the help of function "shift_left.m", which is the third listing below.

Listing 1: eye_gen.m

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                          eye_gen.m                                          %
%                                                                             %
%     this MATLAB program generates an eye diagram from                      %
%     the measured gain (magnitude and phase of s21) of                       %
%            the second 5 GHz bandwidth amplifier                             %
%                    (written by Tom Seniuk)                                  %
%                                                                             %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


%  empty the vectors v_drive, v_filter_orig, and v_filter_freq

v_drive = [];
v_filter_orig = [];
v_filter_freq = [];

%  num_symb = length of the input random bit sequence
%  (in number of bits)
num_symb = 200;

% samps_per_symb = number of samples taken during each bit period
samps_per_symb = 15;

%  bit_rate = self-explanitory (in bits per second)
bit_rate = 10.0 * 10^9;

%  num_points = total number of samples taken of the input random bit
sequence
%  (=number of points in the frequency domain representation of the
%    input random bit sequence, too)
num_points = num_symb * samps_per_symb;

% samp_freq = effective sampling rate of input random bit sequence
required
% in order to achieve samps_per_symb at bit_rate (in samples per second)
samp_freq = bit_rate * samps_per_symb;
```

```
%  T = total time of the bit sequence, in seconds
T = num_symb / bit_rate;

% DT = amount of time between each sample of the input random
% bit sequence, in seconds
DT = 1/samp_freq;

% DF = frequency span between each point in the frequency domain
% representation of the time-domain input random bit sequence
DF = 1/T;

% freq_vec provides an appropriate x-axis for plotting the frequency
% domain representation of various signals
freq_vec = linspace(0.0, samp_freq - 1/T, num_points);

% time_vec provides an appropriate x-axis for plotting the time
% domain representation of various signals
time_vec = linspace(0, T-DT, num_points);

%  this routine creates v_drive, the time-domain, sampled input signal
%  (=strings of 1's and 0's)
for m=1:num_symb
  weight=round(rand);
  symb_vec=weight*ones(samps_per_symb,1);
  v_drive=[v_drive;symb_vec];
end;

%  Plot routine for input bit sequence (=v_drive)

figure
plot(time_vec, v_drive);
axis([-1.0 * 10^(-9)  T+1.0 * 10^(-9) -0.1 1.1]);
xlabel('time, in seconds');
ylabel('amplitude');
title('Input Bit Sequence');

% v_filter_orig = the s-parameters, in polar form (mag & phase, in
degrees)
% of the amp--from 0.0 Hz to 10.0 GHz, in 250.0 MHz steps
v_filter_orig = [1.0+173i 16.0+143i 15.7+110i 15.7+77.5i 16.1+39i
16.5+4i 16.8-32i 16.9-69i 16.9-106i 16.6-143i 15.9-183i 15.9-220i 15.5-
254i 15.4-291i 15.6-327.5i 16.25-366i 16.5-404.5i 16.6-445i 16.9-490i
15.8-538i 13.1-583i 10.3-624.5i 8.45-662i 6.9-698i 5.7-735i 4.4-769i
3.5-800i 2.7-828i 2.3-851i 2.1-881i 2.0-905i 2.0-932i 2.1-960i 2.2-991i
2.2-1022i 2.4-1054.5i 2.3-1090i 2.5-1125i 2.6-1160i 2.6-1196i 2.7-
1236i];

%  f_filter_orig = the frequency points at which s21 was measured
f_filter_orig = linspace(0.0, 10.0 * 10^9, 41);

% this routine takes the measured s21, with its fixed frequency points
% (= v_filter_orig) and creates another s21 with frequency spacing = DF
% (= v_filter_freq), which will then be multiplied by v_drive_freq to
% obtain the frequency domain representation of the input random bit
% sequence after passing through the amplifier.  This is achieved by
% linearly interpolating the magnitude and phase of the measured s21.
v_filter_freq(1) = 1.0;
```

```
n = 2;
k = 2;
f_orig = 250.0 * 10^6;
f = DF;

while n < 42

  v_filter_freq(k) = v_filter_orig(n-1) + (v_filter_orig(n) -
v_filter_orig(n-1)) / (250.0 * 10^6) * (f - (f_orig - 250.0 * 10^6));

  k = k + 1;

  f = f + DF;

  if f > f_orig
    n = n + 1;
    f_orig = f_orig + 250.0 * 10^6;
  end
end

%
f_filter_freq = linspace(0.0, f-DF, (f / DF));

% log magnitude plot of v_filter_orig and v_filter_freq
% (both in polar form right now)
figure
plot(f_filter_orig, 20.0 * log10(real(v_filter_orig)), 'go',
f_filter_freq, 20.0 * log10(real(v_filter_freq)), 'g+');
axis([0.0 10.0 * 10^9 0.0 30.0]);
xlabel('frequency, in Hz');
ylabel('magnitude, in dB');
title('Log Magnitude Plot of Amplifier Response');

% converting v_filter_orig and v_filter_freq from polar to
% rectangular form now...

real_v_filter_freq = real(v_filter_freq) .*
cos(imag(v_filter_freq)*pi/180);
imag_v_filter_freq = real(v_filter_freq) .*
sin(imag(v_filter_freq)*pi/180);

v_filter_freq = real_v_filter_freq + imag_v_filter_freq * 1.0i;

real_v_filter_orig = real(v_filter_orig) .*
cos(imag(v_filter_orig)*pi/180);
imag_v_filter_orig = real(v_filter_orig) .*
sin(imag(v_filter_orig)*pi/180);

v_filter_orig = real_v_filter_orig + imag_v_filter_orig * 1.0i;

%  ...now, take v_filter_freq, lengthen it to match v_drive_freq by
%  padding it with zeros, and conjugately mirror it about samp_freq/2
Y = length(v_filter_freq);

pad = zeros(1, num_points - 2.0 * Y);

v_filter_freq = [v_filter_freq pad];
```

```
for m=1:Y;
  v_filter_freq = [v_filter_freq conj(v_filter_freq(Y+1-m))];
end;

%  v_output_freq = ...well, you can see it for yourself:  it's the
%  frequency domain representation of the amplifier output when driven
%  by the random digital input signal.
v_output_freq = v_drive_freq .* v_filter_freq';

%  plot routine for showing the output waveform
%  (real(v_output) is used to truncate the small amount
%   of imaginary component in v_output, which is due to
%   round-off error during calculation)

min_v = min(v_output);
max_v = max(v_output);
figure;
plot(time_vec, v_output);
axis([-1.0 * 10^(-9) time_vec(num_points)+1.0 * 10^(-9) min_v-0.5
max_v+0.5]);
xlabel('time, in seconds');
ylabel('amplitude');
title('Time Domain Representation of the Output Waveform');


signal = v_output;

%  show_eyeB is the canned function that takes the output
%  waveform vector, "signal", and forms the eye diagram
%  (Big Thanks to Sheldon Walklin)

show_eyeB(samps_per_symb, 2, signal, bit_rate)
```

Listing 2: show_eyeB.m

```
% function to show eye diagram
%
%
% Input Parameters:
%     samps_per_symb - number of samples per symbol
%           num_eyes - number of eyes to display
%           signal - column vector containing signal time record
%
% Returned Values: None
%

function show_eye(samps_per_symb, num_eyes, signal, bit_rate)


disp('Building eye diagram...');
m=size(signal,1);                          % number of rows in signal
vector
traces=floor(m/samps_per_symb);                  % number of traces to
plot
trunc_points=4*samps_per_symb+1;                 % truncated number of
points to plot in eye diagram
x=linspace(0,4,trunc_points);
```

```
x = x .* (num_eyes / bit_rate / 2.0);                    % normalized
abscissa range (abscissa will show symbol number)
eyeh=figure;
max_y=max(signal);                                  % maximum vaue in signal
array
min_y=min(signal);                                  % minimum value in
signal array
axis([0 num_eyes/bit_rate min_y max_y]);                 % set and fix x/y
axis range
hold on;
axis(axis);                                      % freeze axis range for
overlapping plots
signal_trunc=signal(1:trunc_points);                     % truncated signal
for eye diagram plots

for count=1:traces,                                 % plot successive traces
in eye diagram
      plot(x,signal_trunc,'g');
      signal=shift_left(signal,samps_per_symb);          % shift signal
array by samps_per_symb for next plot
      signal_trunc=signal(1:trunc_points);               % tuncated signal
for eye diagram plots
end;

xlabel('Time, in seconds');
ylabel('Normalized Amplitude');
title('Eye Diagram');
disp('Eye diagram complete');

return;
```

Listing 3: shift_left.m

```
%
% Left circular Shift of elements in a column vector.
% (written by Sheldon Walklin)
%
% Parameters:
%          A - vector to apply circular left shift to
%          n - amount of shift (integer)
%
% Returned Values:
%         Y - circular shifted vector
%

function Y=shift_left(A,n)

points=size(A,1);

Y=[A(1+n:points);A(1:n)];

return;
```